1600 W Titanium server power supply with 600 V CoolMOS™ G7 in DDPAK and digital control by XMC™

EVAL_1K6W_PSU_G7_DD

About this document

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Scope and purpose

This document introduces a complete Infineon system solution for a 1600 W server PSU which achieves 80Plus Titanium standard. The EVAL_1K6W_PSU_G7_DD board is a server power composed of a Continuous Conduction Mode (CCM) bridgeless Power Factor Corrector (PFC) with bi-directional switch and a half-bridge LLC DC-DC resonant converter. This document shows the board using CoolMOS™ MOSFETs and CoolSiC™ Schottky diodes in a top-side cooled SMD package (DDPAK) as well as the specifications and the main results obtained during the test of the 1600 W server PSU.

The Infineon components used in the 1600 W server PSU are:

- 600 V CoolMOS™ G7 superjunction (SJ) MOSFET and 650 V CoolSiC™ G6 Schottky diode
- 40 V OptiMOS™ 6 MOSFET
- 1EDI20N12AF isolated and 2EDN7524F non-isolated gate drivers (EiceDRIVER™)
- XMC1402 and XMC4200 microcontrollers
- ICE2QR2280G CoolSET™ Quasi Resonant (QR) flyback controller

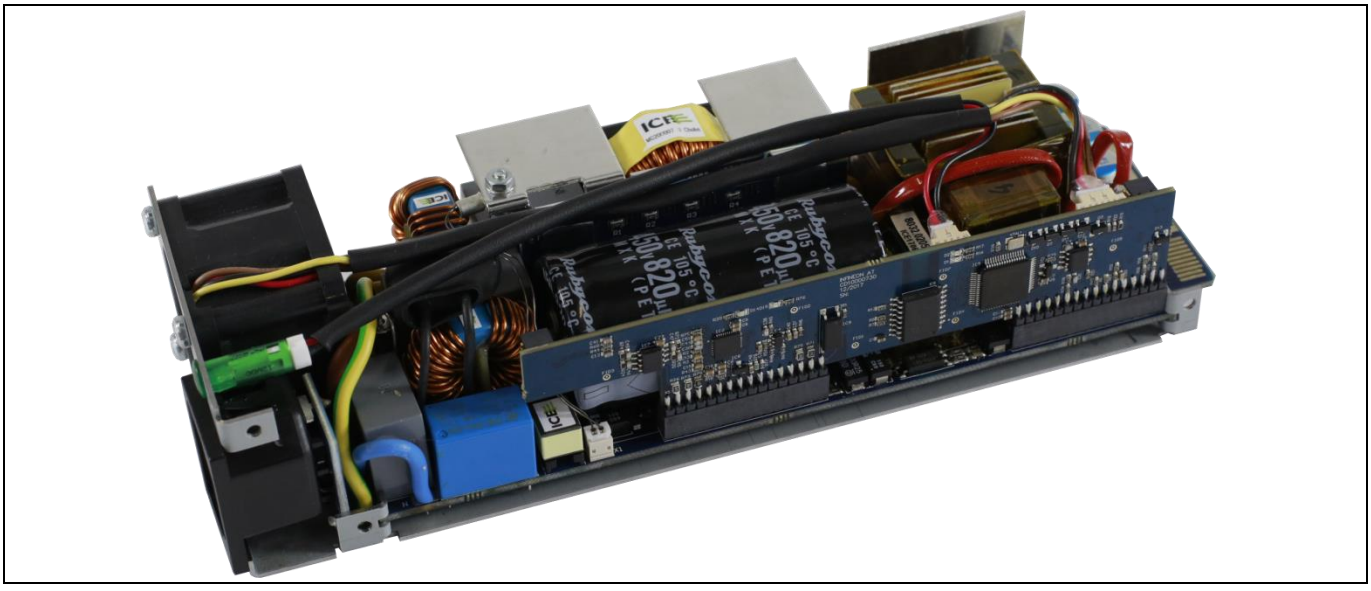


Figure 1 1600 W Titanium server power supply

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1 Background and system description

The trend in SMPS in recent years has been toward increased power density with optimized cost. Achieving this higher power density, high efficiency is a key parameter, since heat dissipation must be minimized. The 800 W server PSU developed with Infineon [1], [2] is a good example of the achievable efficiency levels, out-performing 80Plus Platinum efficiency.

However, if higher power is needed with the same form factor, thus increasing the power density, even higher efficiency is required to further reduce the heat dissipation and make the design thermally feasible.

Keeping this in mind, this document introduces a 1600 W server PSU which complies with 80Plus Titanium efficiency, as shown in Figure 2. The 1600 W PSU keeps the same form factor as the previously presented 800 W server PSU. Therefore, the power density is increased to 44 W/in^3 in the design shown.

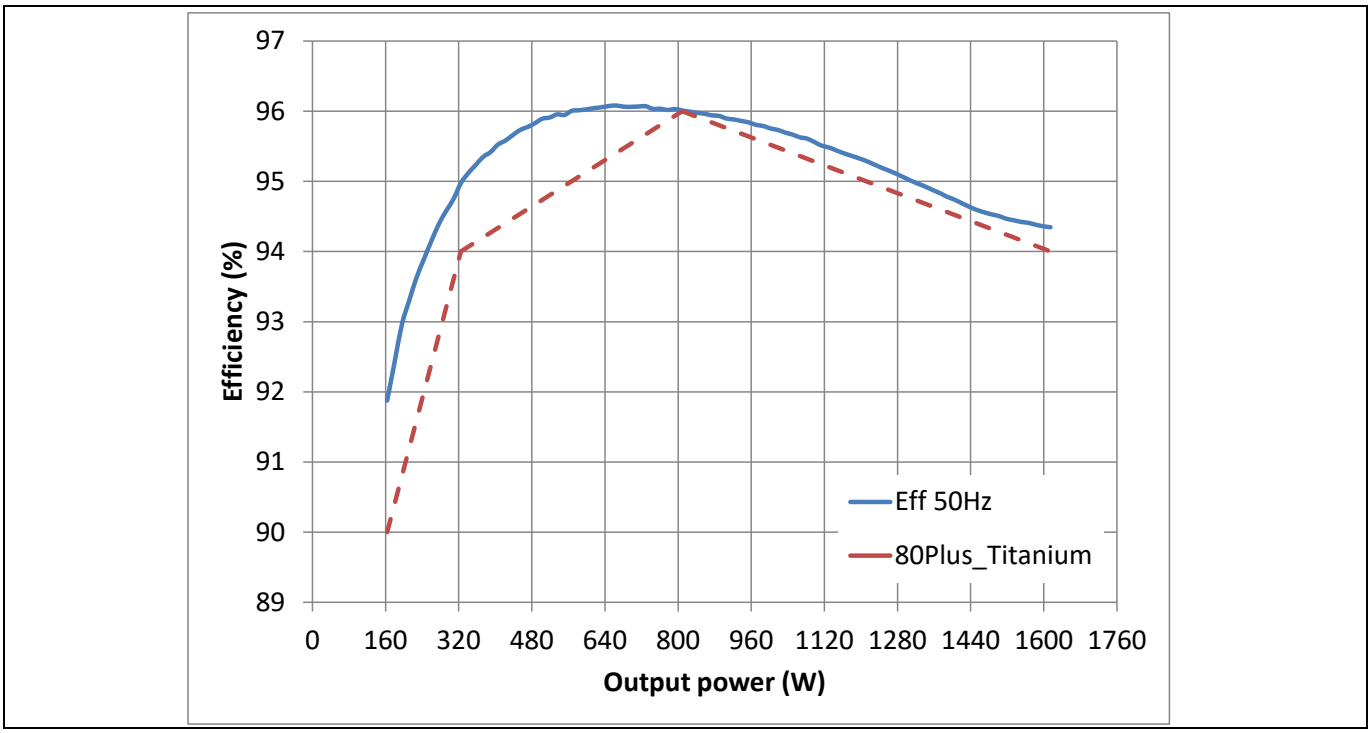


Figure 2 Measured efficiency of the 1600 W server PSU, complying with the Titanium efficiency standard

The efficiency shown can be achieved by using the best-in-class 600 V CoolMOS™ G7 together with 650 V CoolSiC™ G6 Schottky diodes. The outstanding performance of these semiconductor technologies, together with the innovative DDPAK SMD package with top-side cooling, enables a different system thinking, as further presented in [3] and explained in this application note. Due to production variations, efficiency variations in the range of 0.1 percent to 0.2 percent can be seen in the result shown.

The 1600 W server PSU is a system solution (PFC + LLC) developed with Infineon power semiconductors as well as Infineon drivers and microcontrollers. The Infineon devices used in the implementation of the 1600 W server PSU are:

- 150 mΩ 600 V CoolMOS™ G7 (IPDD60R150G7) and 8A 650 V CoolSiC™ G6 Schottky diodes (IDDD08G65C6), all with DDPAK package, for PFC
- 50 mΩ 600 V CoolMOS™ G7 DDPAK package (IPDD60R050G7) and 7 mΩ 40 V OptiMOS™ 6 in Super SO-8 package (BSC007N04LS6) for LLC

- 0.7 mΩ 40 V OptiMOS™ 6 in Super SO-8 package (BSC007N04LS6) as O-ring switch
- 1EDI20N12AF isolated and 2EDN7524F non-isolated gate drivers (EiceDRIVER™)
- ICE2QR2280G QR flyback controller with integrated 800 V CoolMOS™ for the bias auxiliary supply
- XMC1402 (PFC) and XMC4200 (LLC) microcontrollers for control implementation

This document will describe the system and board of the 1600 W server SMPS, as well as the specifications and main test results. For further information on Infineon semiconductors see the Infineon website, as well as the Infineon evaluation board search, and the different websites for the different implemented components:

- CoolMOS™ power MOSFETs
- OptiMOS™ power MOSFETs
- CoolSiC™ Schottky diodes
- Gate driver ICs
- QR CoolSET™
- XMC™ microcontrollers

1.1 System description

The EVAL_1K6W_PSU_G7_DD design consists of a bridgeless PFC with bi-directional switch [4] as the AC-DC stage and a half-bridge LLC with Synchronous Rectification (SR) as the DC-DC stage (Figure 3). The power supply has been designed to comply with the requirements of a data center server operation.

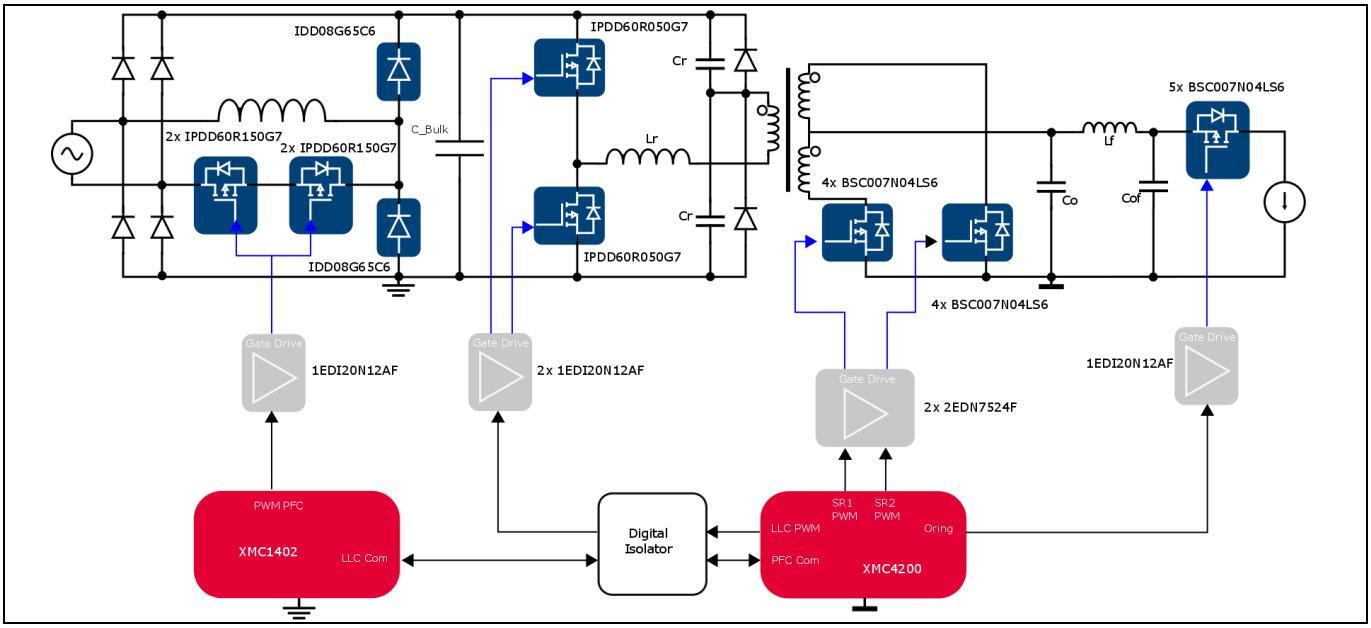


Figure 3 1600 W Titanium server PSU (EVAL_1K6W_PSU_G7_DD) – simplified diagram showing the topologies implemented and the Infineon semiconductors used

The PFC stage is operated exclusively at high-line (176 Vrms minimum, 230 Vrms nominal) in CCM with a 65 kHz switching frequency. The bulk capacitance is designed to comply with the hold-up time shown in Table 1. The PFC function to achieve bulk voltage control at an adequate level for the DC-DC converter, while demanding high-quality current from the grid, is implemented in an Infineon XMC1402 microcontroller. Further detail on PFC control implementation in the XMC™ 1000 family can be found in the application notes of other Infineon PSU and PFC evaluation boards [1], [2], [5], [6].

The DC-DC stage is an LLC resonant topology with center-tapped transformer and SR. The resonant frequency of the implemented resonant tank is 160 kHz and the operating switching frequency is allowed to move in the range from 52 kHz to 300 kHz. The targeted output voltage is 12.2 V with a nominal ouput current of 132 A. The LLC control is implemented in an XMC4200 Infineon microcontroller, which includes voltage regulaton, burst mode operation, output Over Current Protection (OCP) and Over Voltage Protection (OVP) and timer configuration for CoolMOS™ and OptiMOS™ safe operation. Further detail about digital control implementation of LLC in the XMC™ 4000 family can be found in [1], [2], [7].

O-ring switches are mounted for efficiency consideration of the full system solution. However, no advance O-ring function is included in the control implementation. Furthermore, an I^2C channel is reserved in the secondary controller, which enables PM-Bus communication.

1.2 Board description

Figure 4 shows a placement of the different sections of the EVAL_1K6W_PSU_G7_DD server PSU with Infineon DDPAK semiconductors. The board shown is 19.3 cm long, with a width of 7 cm and a height of 4.4 cm.

Inmediately after the AC input connector, the fuse and the NTC inrush current limiter are placed together with the input relay, and these are followed by a two-stage EMI filter. In the middle part of the board, the AC-DC stage is placed, including the bulk capacitor. Finally, the DC-DC converter, the O-ring switches and the output connector are placed on the right. In addition, the bias converter generates the required supplies for the driving and control circuitry. The control board is placed along the side of the power supply.

In addition a host board to be connected to the output connector is attached. This board includes power connectors and a sensing point for the output voltage as well as a switch for remote on-off. Furthermore, it offers the possibility of externally supplying the fan, as explained in [1].

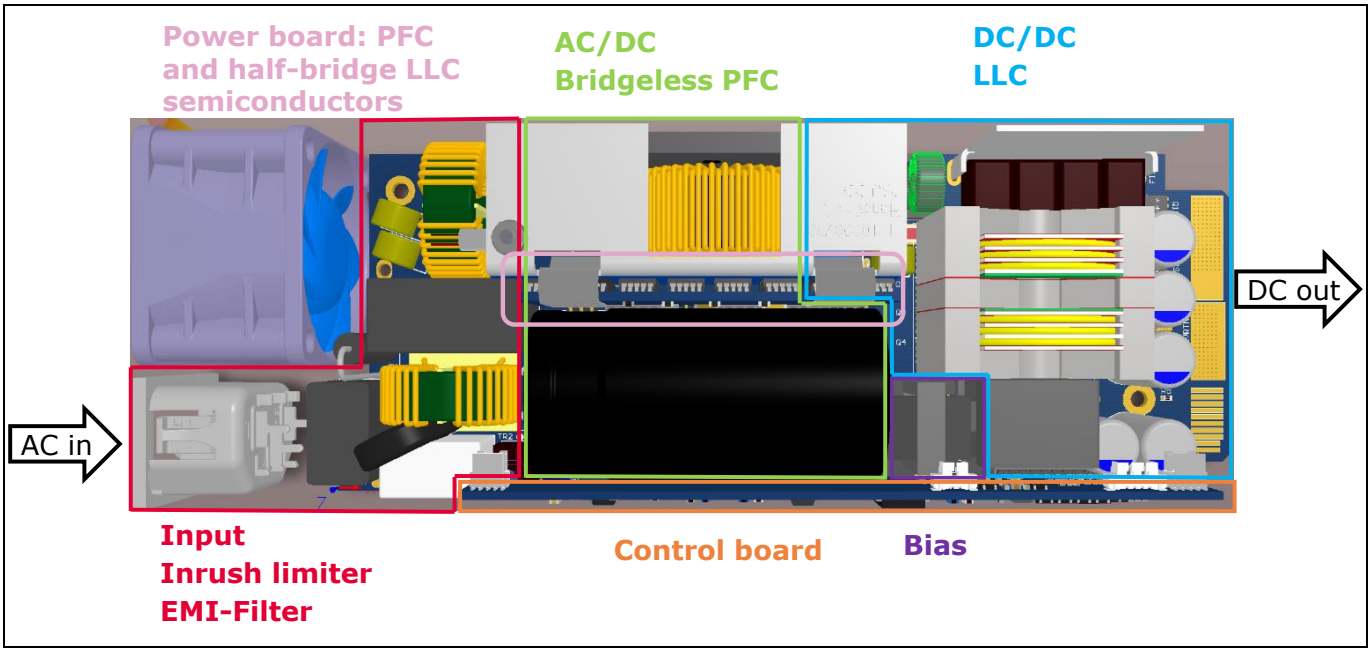


Figure 4 **Placement of the different sections in the 1600 W PSU with Infineon DDPAK CoolMOS™ and CoolSiC™**

1.3 DDPAK power board

The use of the top-side cooled DDPAK package enables different system thinking and the inclusion of SMD packages in high-power SMPS applications [3]. The previously shown placement of the 1600 W PSU is a good example of this system thinking and SMD integration.

The use of CoolMOS™ G7 transistors in both PFC and LLC allows loss reduction due to an E_{oss} and $R_{DS(on)}$ reduction [3]. Furthermore, the forward voltage in the CoolSiC™ G6 diode is reduced, contributing to lower diode losses [3]. The lower losses together with an improved thermal resistance, which compensates the lower dissipation area in respect to leaded packages, and the low profile of the top-side cooled SMD package, enable mounting of the PFC and half-bridge switches to share the same heatsink.

The use of a power board (Figure 5) enables a high power density design, while having optimized commutation loops and, therefore, low parasitic inductances. This power board, which mounts the PFC CoolMOS™ G7 switches and CoolSiC™ G6 Schottky diodes, together with the LLC CoolMOS™ G7 half-bridge switches, is vertically placed in the central part of the PSU in front of the fan (the pink area in Figure 4). In this case, eight parts are soldered to the power board and share the same heatsink, which is attached by using pressure clips as shown in Figure 5.

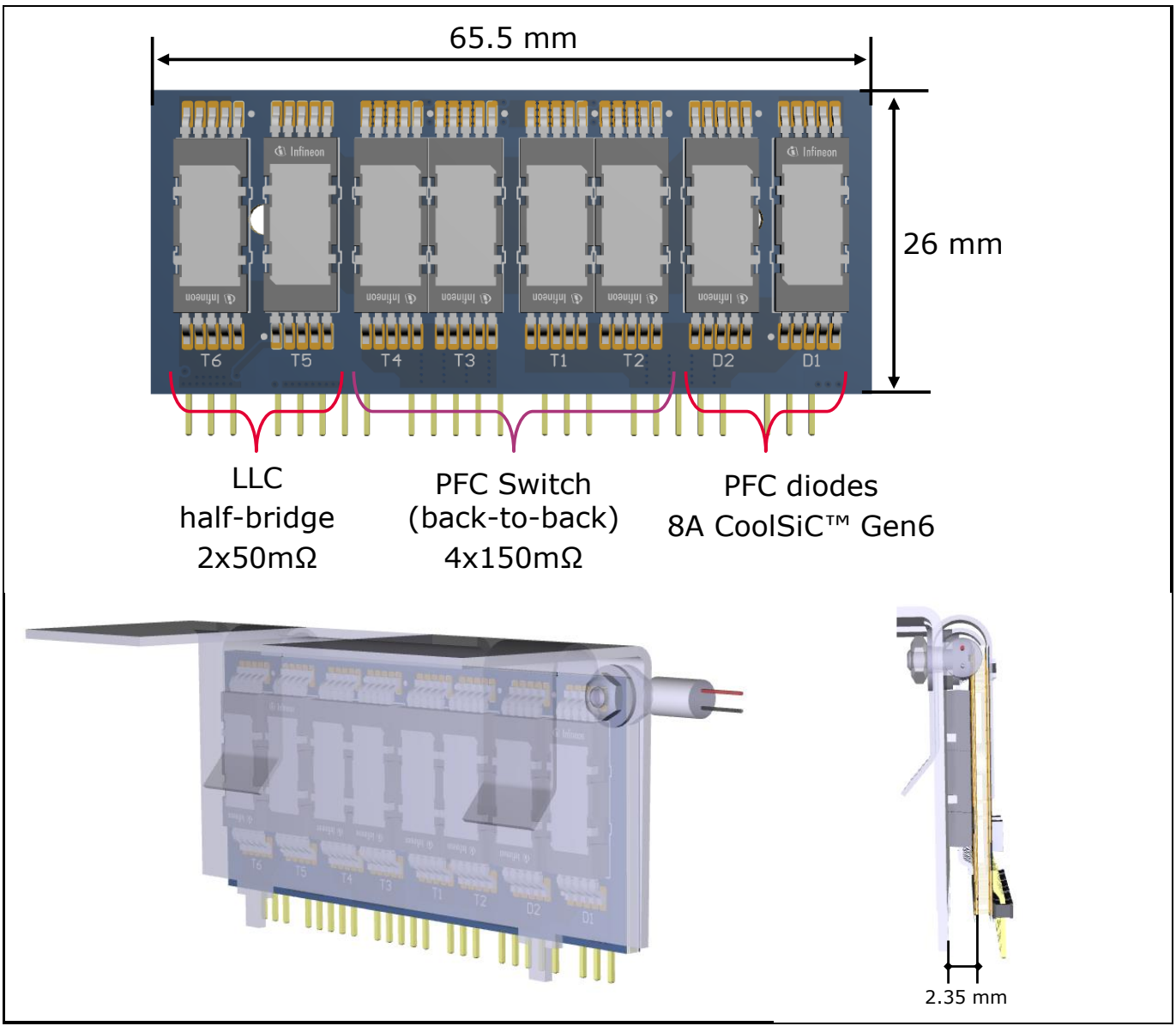


Figure 5 **Power board mounting the Infineon DDPAK semiconductors for the PFC and half-bridge LLC**

2 Specification and test results

This chapter presents the specifications, performance and behavior of the 1600 W server PSU developed using CoolMOS™ G7 in a DDPAK package. Table 1 shows the demonstrator performance and specifications under several steady-state and dynamic conditions.

Table 1 Summary of specifications and test conditions for the 1600 W PSU

Test		Conditions	Specification	
Efficiency test		230 Vrms, 50 Hz/60 Hz, 10 percent to 100 percent load	80Plus Titanium efficiency. η_{pk} = 96 percent at 800 W (50 percent load)	
Current THD		230 Vrms, 50 Hz/60 Hz, 10 percent to 100 percent load	THDi less than 10 percent from 20 percent load	
Power factor		230 Vrms, 50 Hz/60 Hz, 10 percent to 100 percent load	PF more than 0.95 from 20 percent load	
Output voltage			12.2 V	
Steady-state V_{out} ripple		230 Vrms, 50 Hz/60 Hz, 10 percent to 100 percent load	$\lvert\Delta V_{out}\rvert$ less than 120 mV_{pk-pk}	
Inrush current		230 Vrms, 50 Hz/60 Hz, measured on the first AC cycle	I_{in_peak} less than 30 A	
Power line disturbance	AC lost (hold-up time)	230 Vrms, 50 Hz, 10 ms at 100 percent load, 20 ms at 50 percent load	$\lvert\Delta V_{out}\rvert$ less than 240 mV_{pk}	No damage: * PSU soft-start if bulk voltage under 310 V * PSU soft-start if V AC out of range for certain time
	Voltage sag	200 Vrms, 50Hz/60Hz, different sag conditions, 100 percent load		
Brown-out			174 V on; 168 V off	
Load transient		1 A ↔ 66 A, 0.5 A/µs	$\lvert\Delta V_{out}\rvert$ less than 240 mV_{pk}	
		66 A ↔ 133 A, 0.5 A/µs		
OCP		30 s at 141 A	LLC off Resume of operation requires bulk voltage to drop under 310 V	
		10 s at 149 A		
		1 ms at 168 A		
		Output terminals in short-circuit	Detection within switching cycle. Resumption of operation requires bulk voltage to drop under 310 V	
EMI conducted		230 Vrms, 50Hz, full load, resistive load, lab set-up	Complies with Class B limits	

2.1 Performance and steady-state waveforms

In this chapter the steady-state waveforms are presented together with the efficiency and the Power Factor (PF) and THD achieved in the 1600 W server PSU presented in this application note. The PSU operates only in high-line (from 176 V to 265 V line voltage) with a nominal input voltage of 230 Vrms. Therefore, the efficiency is presented for this nominal voltage. As shown in Figure 6, the Infineon 1600 W PSU with DDPAK CoolMOS™ G7 and CoolSiC™ G6 achieves Titanium efficiency.

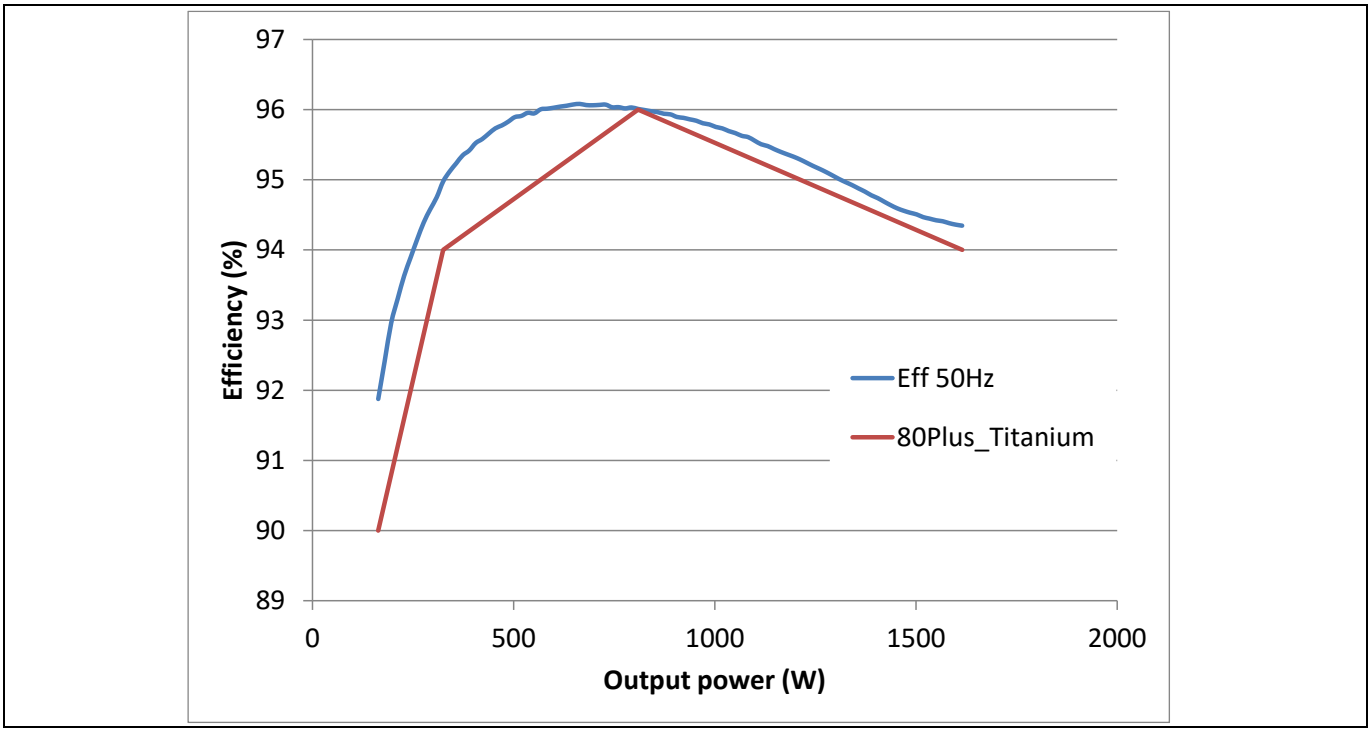


Figure 6 Measured efficiency at 230 V 50 Hz input voltage

Figure 7 depicts the measured PF and THD. The achieved PF is over 0.95 when the output power is higher than the 20 percent of the nominal output power, i.e. 320 W, for both 50 Hz and 60 Hz input voltage. In the case of the THD, the distortion is under 10 percent for output power over the 20 percent level for both 50 Hz and 60 Hz input voltage.

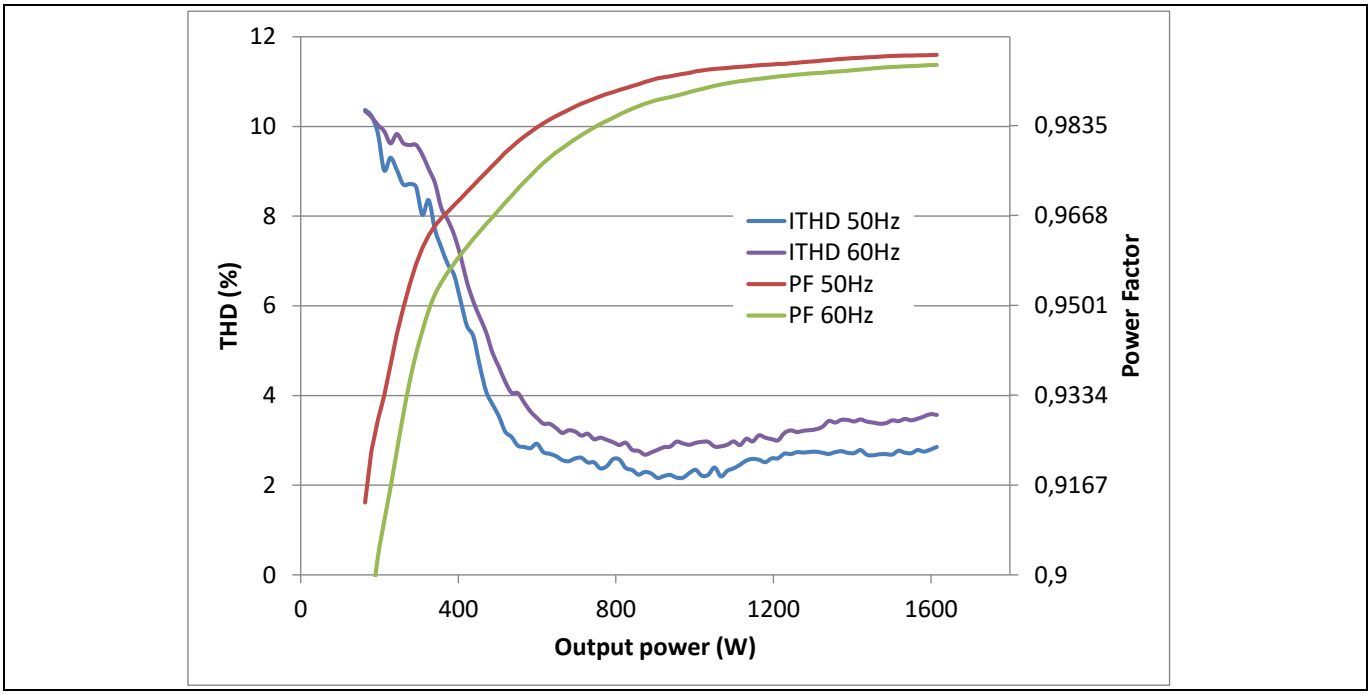


Figure 7 Measured THD and power factor at 230 V input voltage for both 50 Hz and 60 Hz

The main waveforms of the PSU are presented for different output power levels for 50 Hz (Figure 8) and 60 Hz (Figure 9) at nominal input voltage. As it can be seen, the input current presents low distortion according to the previously presented curve and the output voltage ripple is under the specified ±120 mV range.

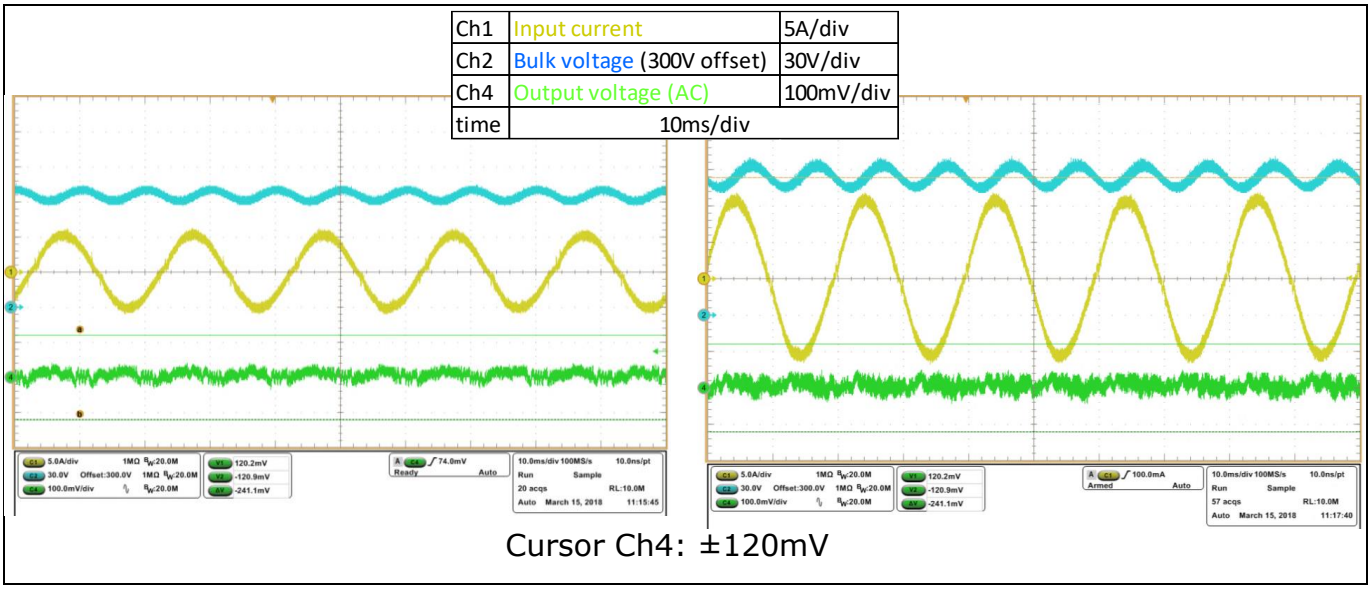


Figure 8 Steady-state waveforms at 230 V 50 Hz for 50 percent load (left) and 100 percent load (right)

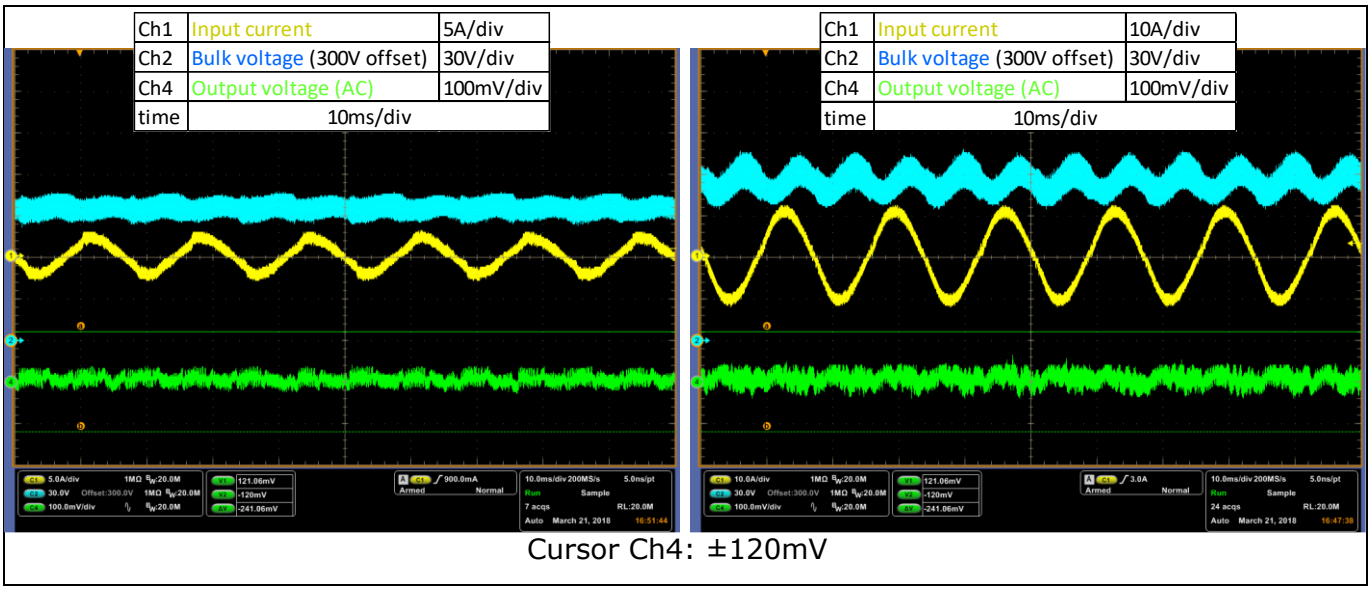


Figure 9 Steady-state waveforms at 230 V 60 Hz for 20 percent load (left) and 100 percent load (right)

2.2 Inrush current

In the PSU the inrush current when connecting to the AC source is limited with a NTC. This resistor is short-circuited by a parallel relay before start-up if the input and output voltage conditions to start the PFC are met. The inrush current is measured at the first AC cycle and it is independent on the output load. In Figure 10 the full-load start-up of the server PSU is presented and the inrush current is highlighted. According to the measurement the inrush current is significantly under the specified 30 A in Table 1.

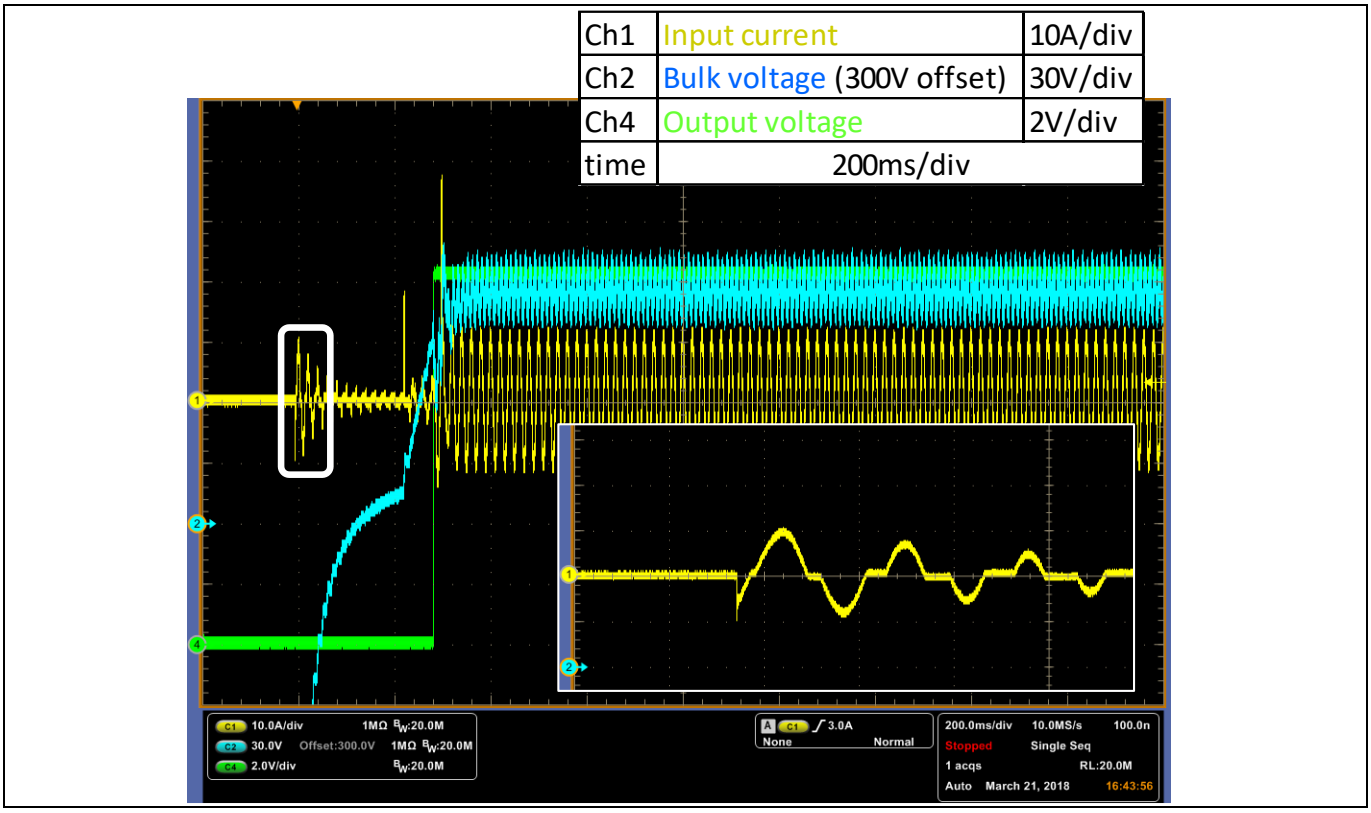


Figure 10 Inrush current of the 1600 W server PSU at full-load start-up

2.3 Power line disturbance

Two main line disturbance conditions can occur when connected to the grid. On one side the AC can be lost during a certain time – Line Cycle Drop Out (LCDO) – and, on the other side, the AC voltage can suddenly decrease to an abnormal value – voltage sag. This section introduces the test conditions for both disturbances as well as the SMPS performance when those conditions are applied using a programmable AC source.

2.3.1 Line cycle drop-out

The 1600 W power supply operates exclusively in high-line. Therefore the AC LCDO capability is tested from 230 V to 0 V. Different timing, related to the specified hold-up time and the line frequency, is applied as shown in Table 2. The test results (Figure 11 and Figure 12) show that the output voltage is within the specified dynamic variation regardless of the start angle of the voltage drop-out. In case the drop-out is longer than specified, output voltage regulation can be lost, and even a turn-off and restart of the unit is possible if the bulk voltage falls to 310 V.

Table 2 Applied voltage cycles for LCDO test at different loads with 50 Hz AC input voltage

		1st to 10th time (100 ms period)	
Applied voltage	230 V AC	0 V AC	230 V AC
Timing at different load conditions	50 percent load	20 percent (20 ms)	80 percent (80 ms)
	100 percent load	10 percent (10 ms)	90 percent (90 ms)

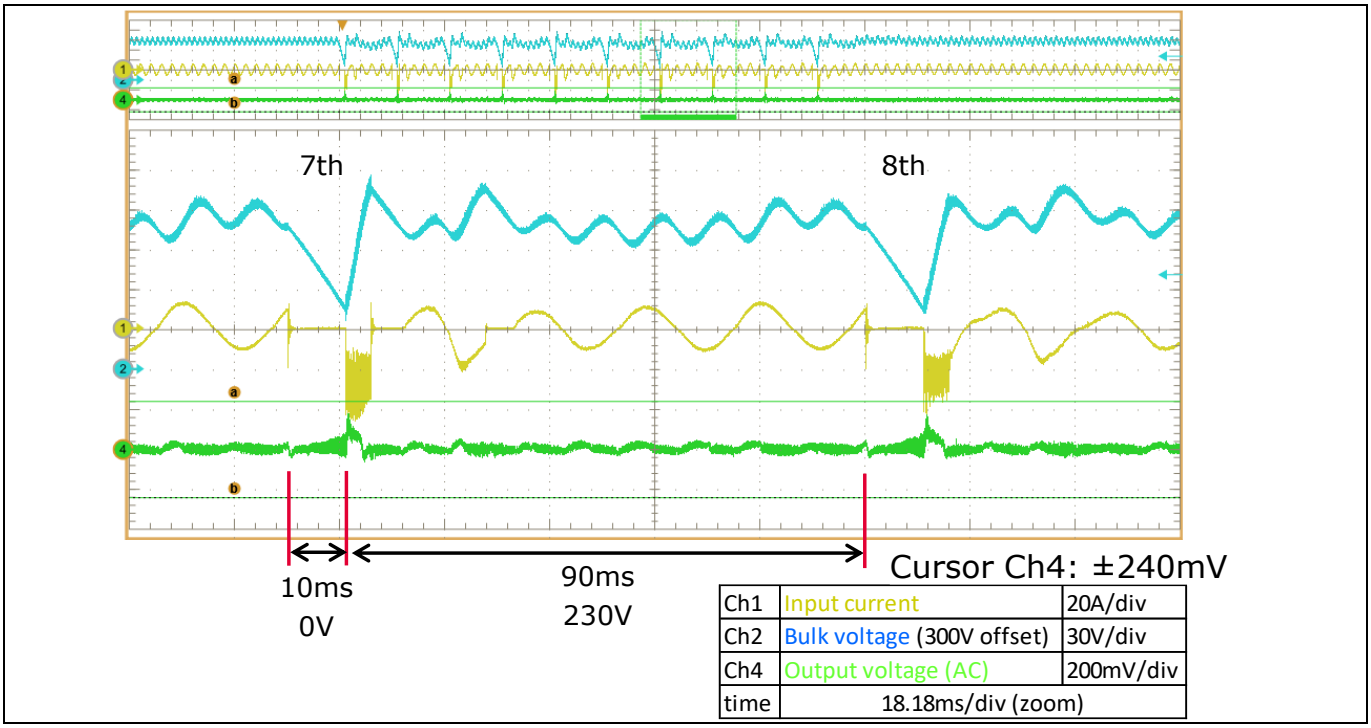


Figure 11 **Detail of the 7th and 8th repetition in a 10 ms LCDO test at 230 V AC, 50 Hz and 100 percent load with a starting angle of 45 degrees**

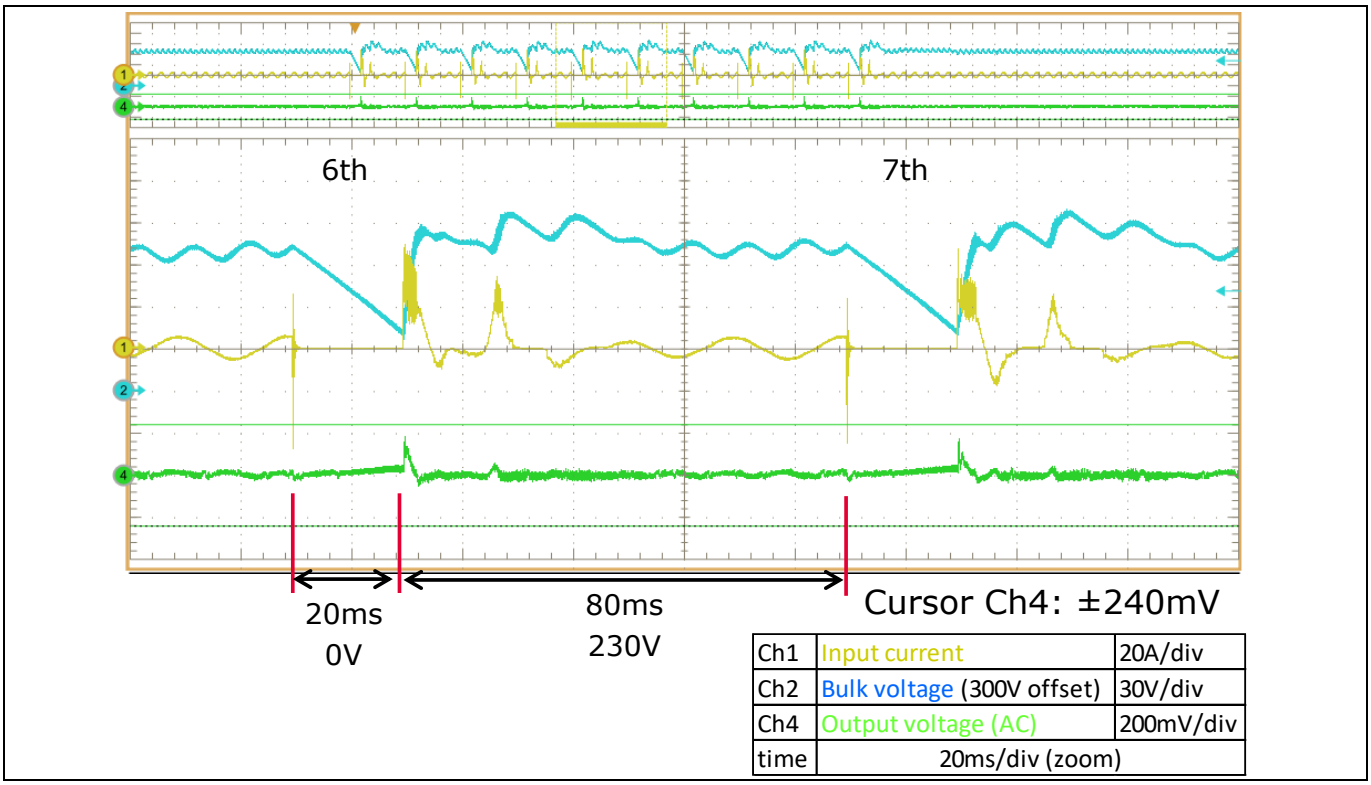


Figure 12 **Detail of the 6th and 7th repetition in a 20 ms LCDO test at 230 V AC, 50 Hz and 50 percent load with a starting angle of 90 degrees**

2.3.2 Voltage sag

For high-line, two different voltage sag conditions (Table 3) are considered and tested. Figure 13 shows the PSU behavior with voltage sag according to Table 3. As can be seen, the output voltage is not affected by the input voltage variation. However, if the voltage sag lasts longer than specified in the table, the power supply turns off and restarts with soft-start after an idle time. Figure 14 shows this behavior when a voltage sag to 150 V is applied for longer than 2s.

Table 3 Voltage sag conditions applied in the 1600 W PSU test

		1st to 10th time	
	Steady AC input	Voltage sag (time)	Period
AC input	200 V AC	130 V AC (0.5 s)	5 s
	200 V AC	150 V AC (2 s)	20 s

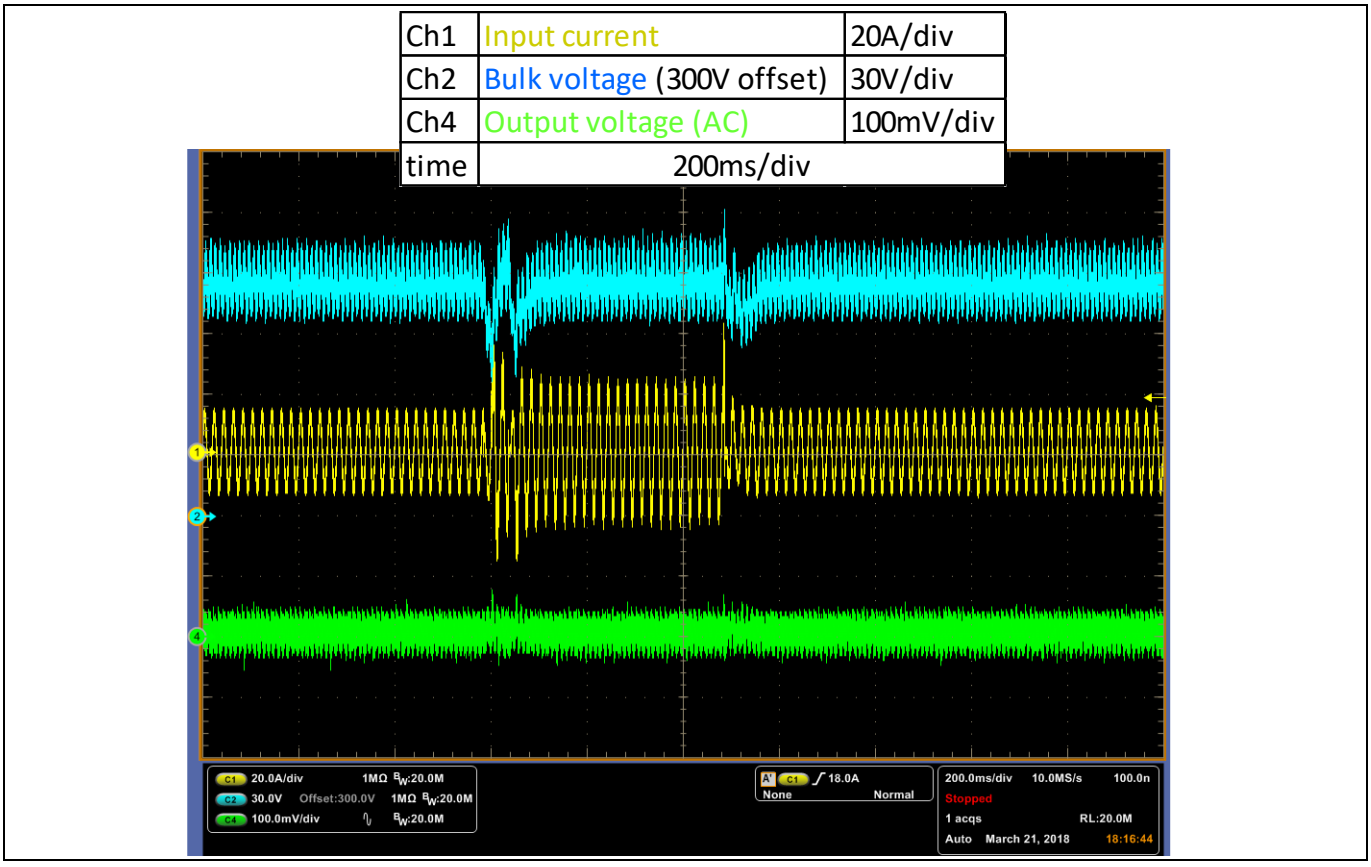


Figure 13 Main waveforms during a 500 ms and 130 Vrms voltage sag at full load

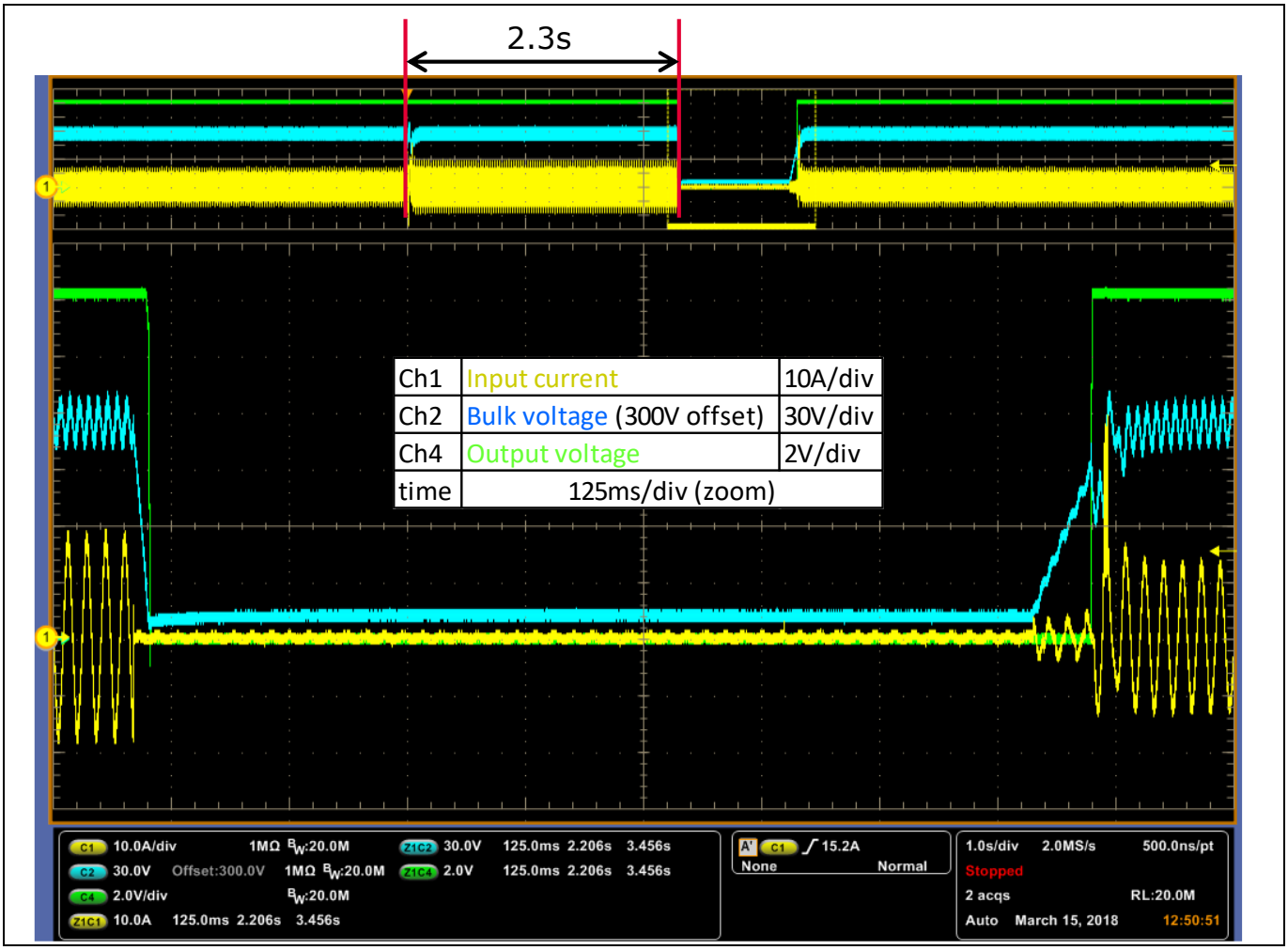


Figure 14 SMPS resumes operation after 150 Vrms voltage sag applied for 3.5 seconds at full load

2.4 Output voltage dynamic behavior

In addition to power line disturbance, two other dynamic perturbances can affect the performance of the power supply shown: load and input voltage variation.

2.4.1 Load transient response

As specified in Table 1, light-load (1 A) to half-load (66 A) and half-load to full-load (132 A) with 0.5 A/µs steps are considered. Figure 15 and Figure 16 show two examples for the different load steps at different frequency ratios. In all the tested cases the output voltage dynamic ripple is within ±240 mV of the steady-state voltage of 12.2 V.

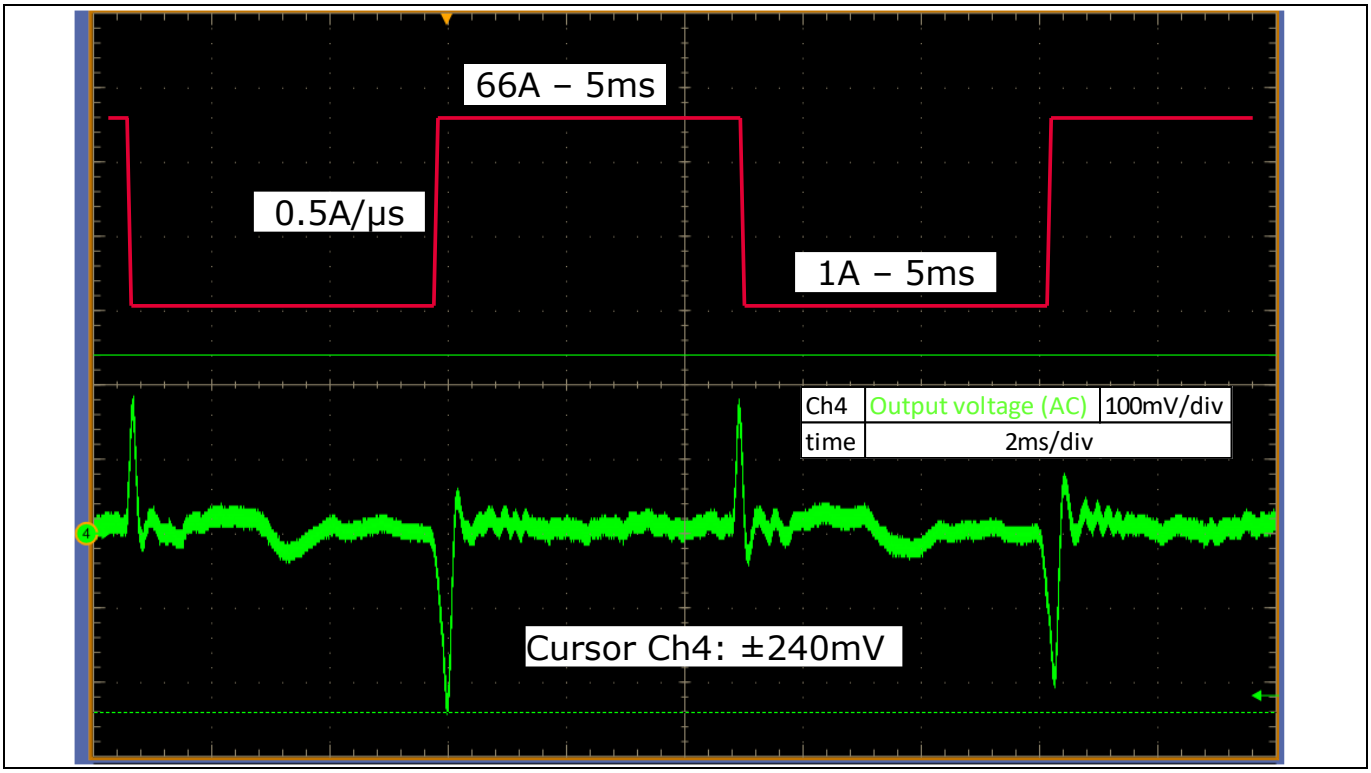


Figure 15 **Output voltage response to 1 A to 66 A dynamic load steps with 0.5 A/µs current slope every 5 ms**

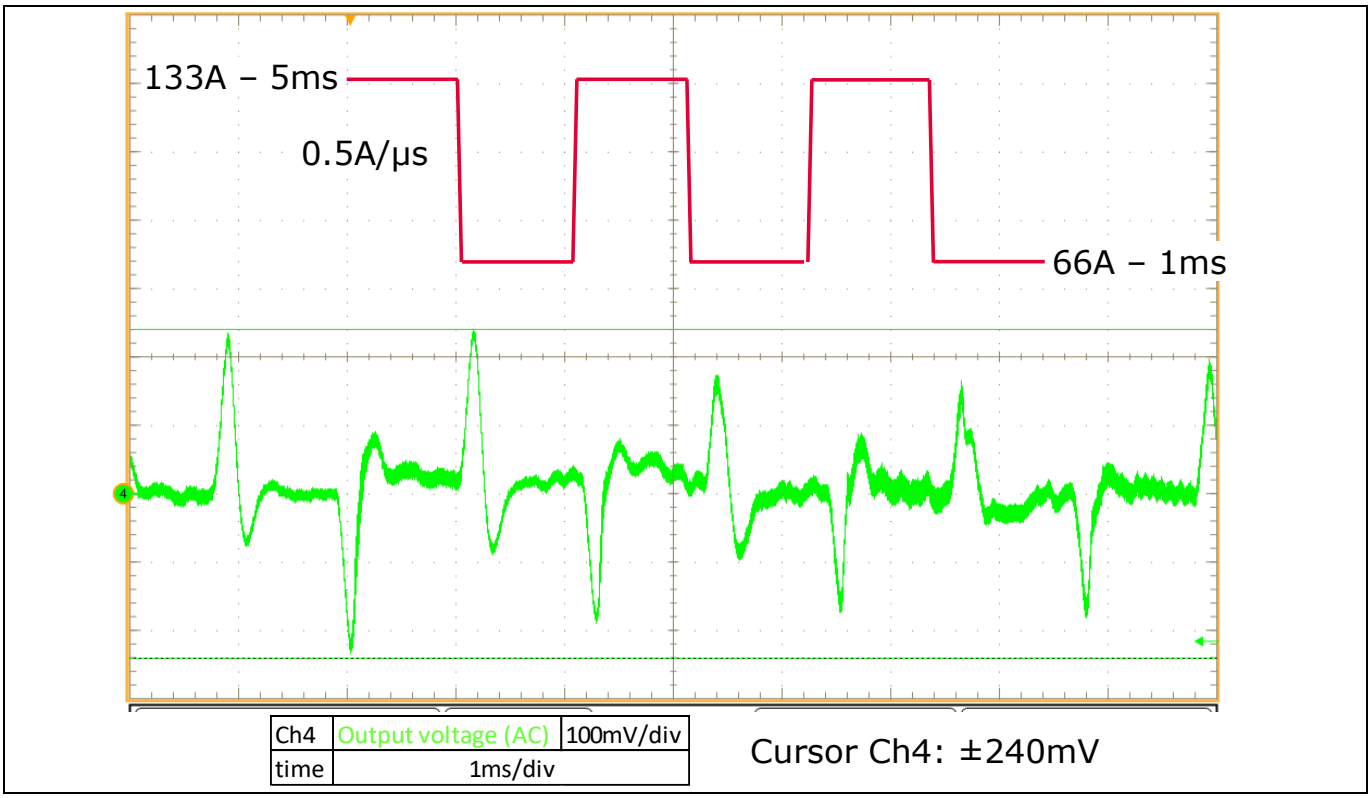


Figure 16 **Output voltage response to 132 A to 66 A dynamic load steps with 0.5 A/µs current slope every 1 ms**

2.4.2 Input voltage variation

Input voltage variations, as seen in the power line disturbance section, modify the bulk voltage and ultimately affect the output voltage ripple. This can occur as well when the input voltage varies even within the normal operation range, as shown in Figure 17.

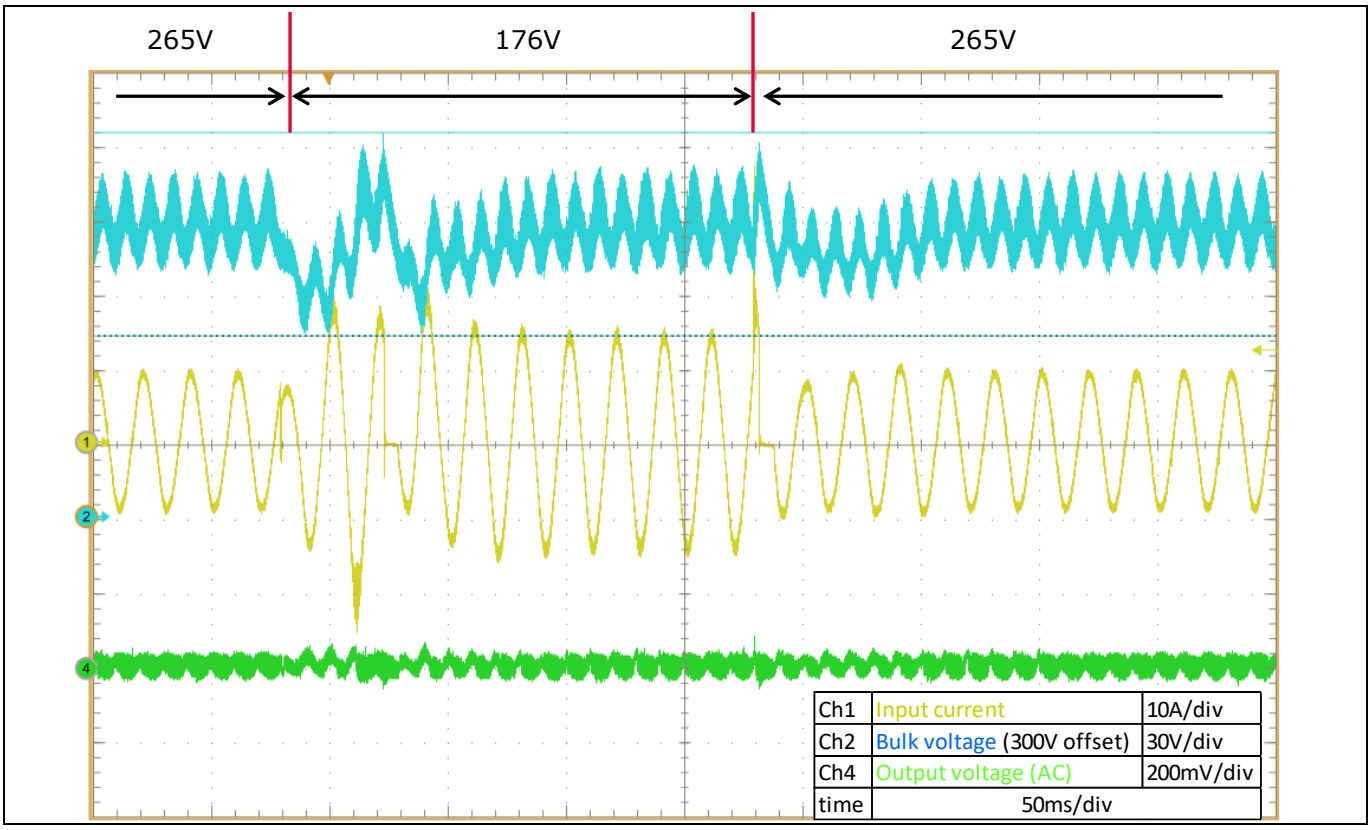


Figure 17 Maximum (265 Vrms) to minimum (176 Vrms) line voltage variation at full-load operation

2.4.3 Burst mode

The DC-DC stage of the 1600 W PSU goes into burst mode operation in light- or no-load conditions, and in those dynamic conditions where the output voltage regulation is lost due to maximum frequency limitation (300 kHz). Figure 18 shows the output voltage ripple for no-load operation of the PSU when the LLC converter is in burst mode.

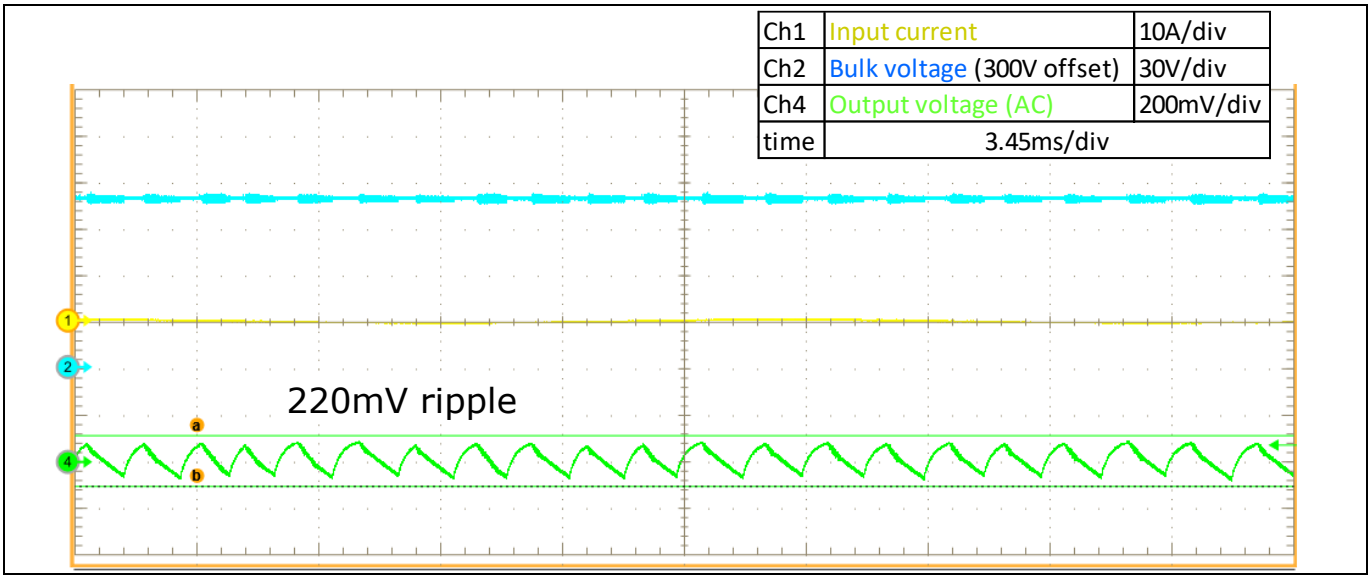


Figure 18 Output voltage ripple in burst mode at no-load operation

2.5 Protections

Both stages in the 1600 W server PSU implement protections to ensure robust and reliable operation.

In the case of PFC, the brown-out protection considers the possible voltage sag as already introduced. Furthermore, average and peak inductor current limitations are implemented as well bulk voltage monitoring for both under- and over-shoot.

Regarding the LLC, apart from switching frequency limitation (52kHz to 300kHz), two main protections are implemented: over-current and over-voltage.

2.5.1 Over Current Protection (OCP)

The programmed OCP levels, together with the maximum allowed time for each level, are introduced in Table 1. Figure 19 shows the unit reaction to a 155 A load current. LLC shuts down and the bulk voltage must go under 310 V to allow a PSU restart.

In addition, a fast short-circuit protection is implemented by comparing the resonant current with a fixed level, set to 56 A. This enables detection of a very heavy over-load within few switching cycles. The power supply can also be restarted when the bulk voltage decreases under 310 V after a short-circuit fault.

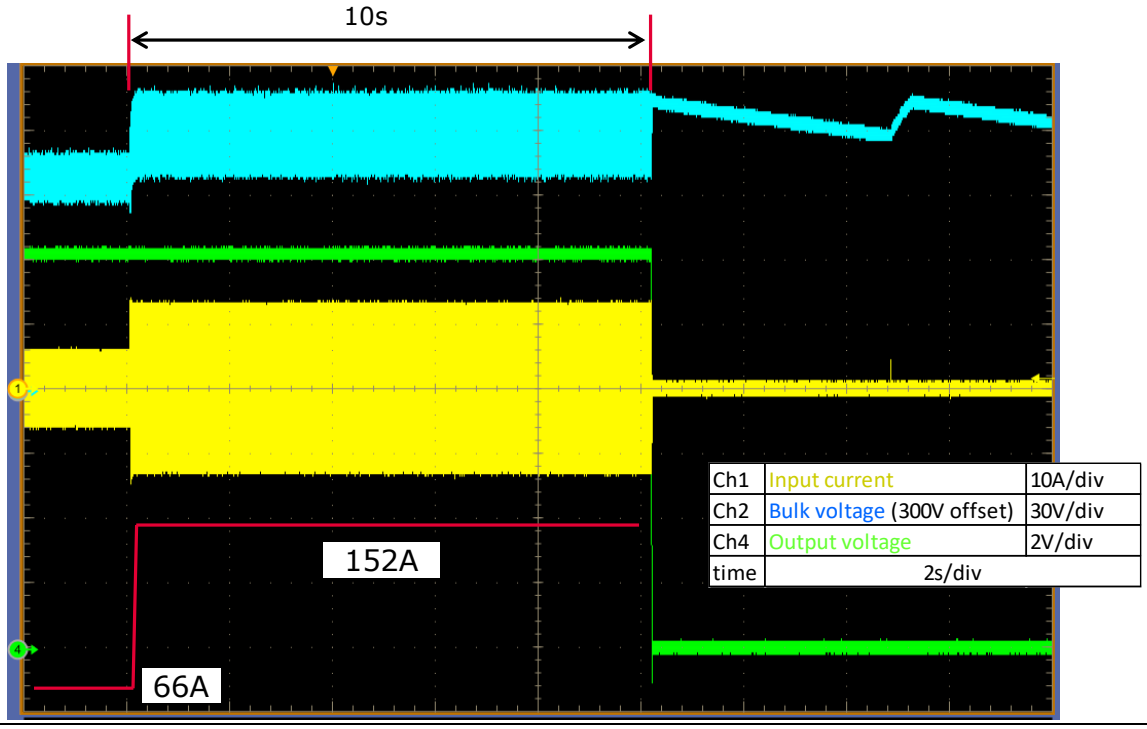


Figure 19 LLC converter of the 1600 W SMPS shut-down due to 155 A OCP

2.5.2 Over Voltage Protection (OVP)

In case of control issues in the DC-DC stage of the power supply, OVP is set to 14 V. Figure 20 shows the mentioned protection when the LLC is operated with a modified control loop, which is allowing the output voltage to reach the OVP level.

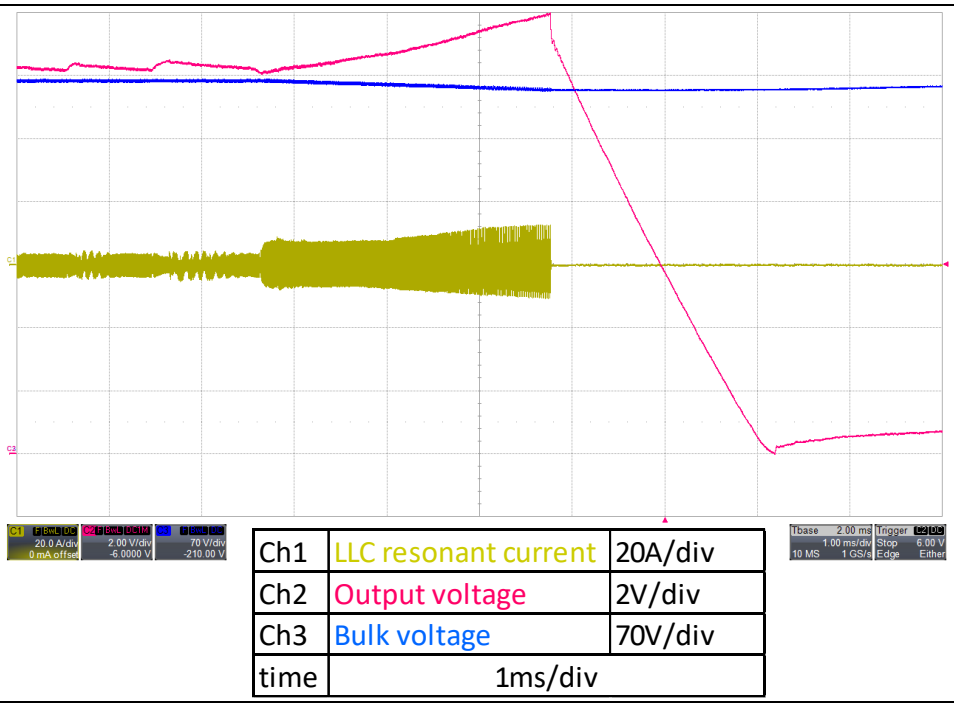


Figure 20 OVP triggered in the PSU with a modified control loop

2.6 Conducted EMI

The high power density 1600 W server PSU with DDPAK includes an EMI filter to comply with the electromagnetic emission standards. In this case the conducted EMI complies with Class B limits as shown in Figure 21. Pure resistive load is used for the conducted EMI test, and the converter runs at nominal output power with nominal (230 V) input voltage at 50 Hz.

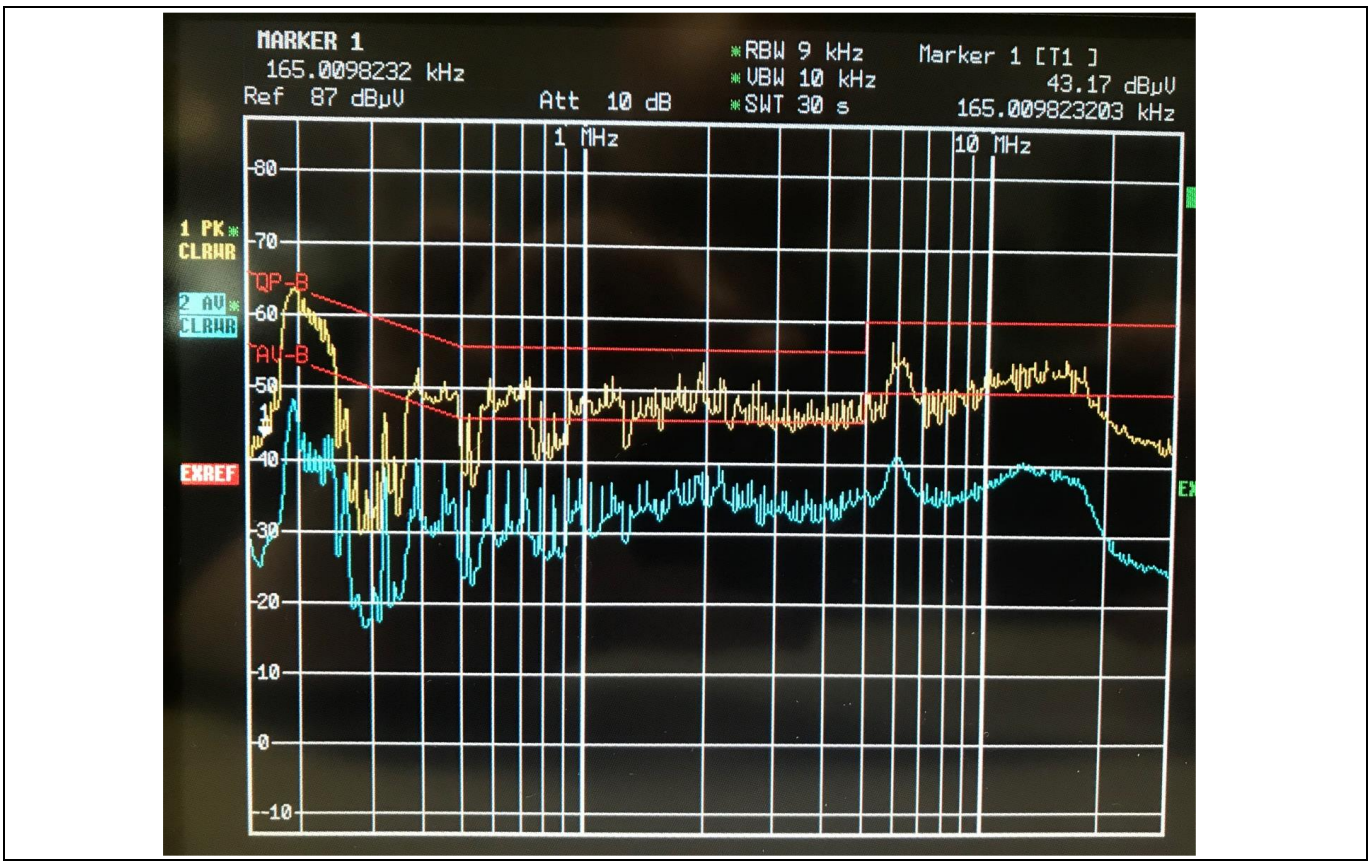


Figure 21 Measured EMI conducted emissions (yellow: quasi-peak, blue: average) at 230 V AC input and 1600 W output resistive load

2.7 Thermal measurements

A long time test has been run with attached Type K thermocouplers to the main devices of the EVAL_1K6W_PSU_G7_DD board. The test has been run for nominal input voltage (230 V_{rms}) as well as the minimum input voltage (176 V_{rms}), which is the worst case for the PFC operation. In both cases, nominal load (132 A at 12.2 V output) has been applied during the test at room temperature. The tested unit was enclosed and the fan was controlled by the secondary side controller and supplied from the server power supply output.

Therefore, the results presented in this section provide the thermal performance of the 1600 W server power supply with Infineon semiconductors introduced in this document at room temperature.

The monitored parts in the thermal test are:

- PFC switch: the four switches have been monitored with similar results. The presented measurement corresponds to the hottest device during the test.
- PFC diode: in this case one of the two SiC diodes has been measured.
- PFC choke
- Diode bridge: current flows through part of the input diode bridge during PFC diode conduction.

- LLC half-bridge
- LLC transformer
- LLC synchronous rectifiers: the measurement of a sampled device from both SR branches is shown.
- Oring switch: as in the SR case, one of the paralleled devices has been sampled in these measurements.

Figure 22 shows the temperature evolution of the sensed points for nominal input and load conditions. It can be seen that the maximum temperature is obtained in the SR due to the high current in the secondary side. The measured maximum temperature is 84°C at room temperature, which provides margin enough in case the ambient temperature increases.

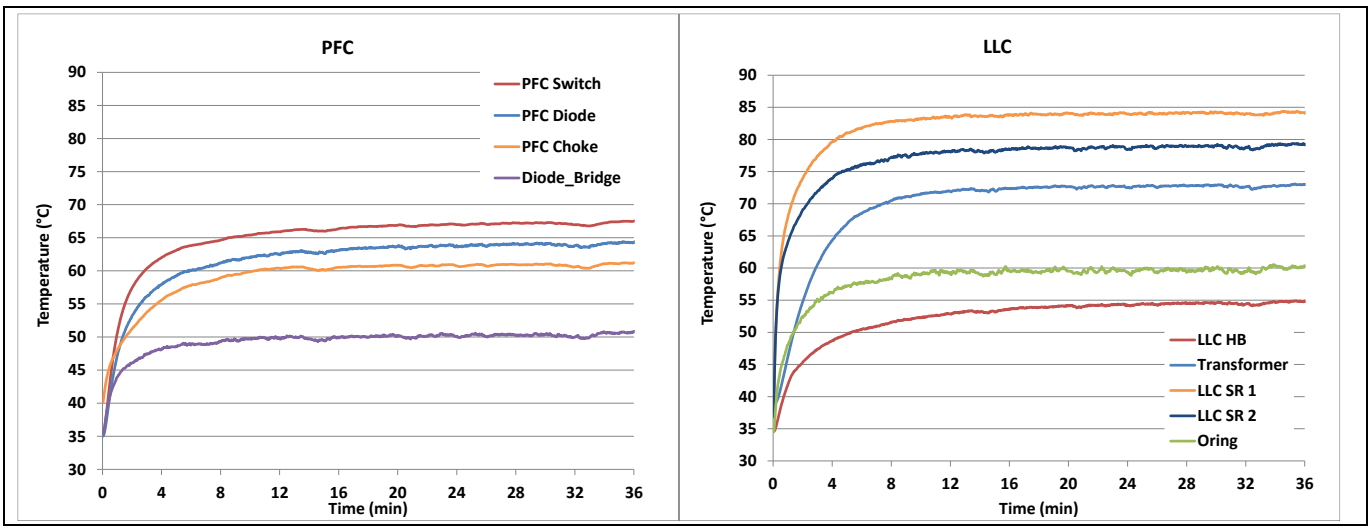


Figure 22 Temperature evolution with operation time in EVAL_1K6W_PSU_G7_DD at nominal input and load conditions, and room temperature.

In the case of minimum input voltage operation (176 V_{rms}) the thermal behavior is presentend in Figure 23. The LLC temperatures are very consistent with the presetend for nominal conditions, since the PFC is regulating the bulk voltage for the DC to DC converter. However, the measured temperatures in the PFC section have increased considerably in respect to the nominal input voltage. This temperature increase is due to the higher input current for the reduced input voltage. Nevertherless, despite the PFC choke is the hot spot of the power supply, together with the SR, the maximum temperature is the same than presented before and there is still margin for higher ambient temperature operation.

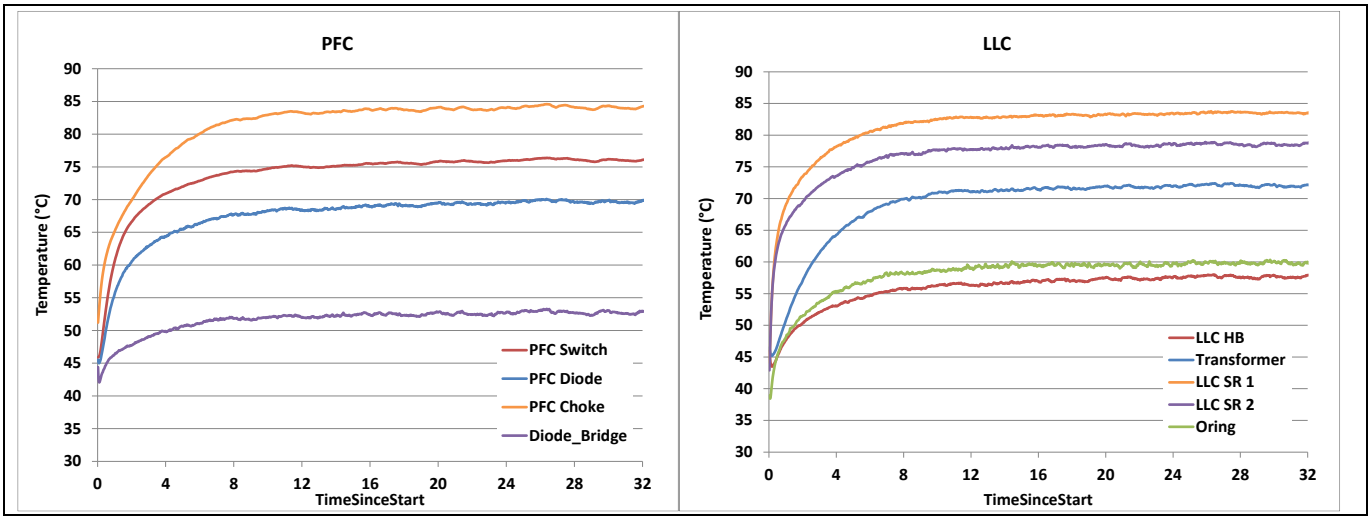


Figure 23 Temperature evolution with operation time in EVAL_1K6W_PSU_G7_DD at minimum input and nominal load conditions, and room temperature.

3 PFC control implementation

The AC-DC stage of this 1600W power supply performs power factor correction by a digital implemention of an average current control. Figure 24 shows the control block diagram which correspond to a typical two loop approach, with line feedforward, used in average current control. The presented blocks are implemented in software (SW). Figure 24 includes as well more detail on the implemented algorithms.

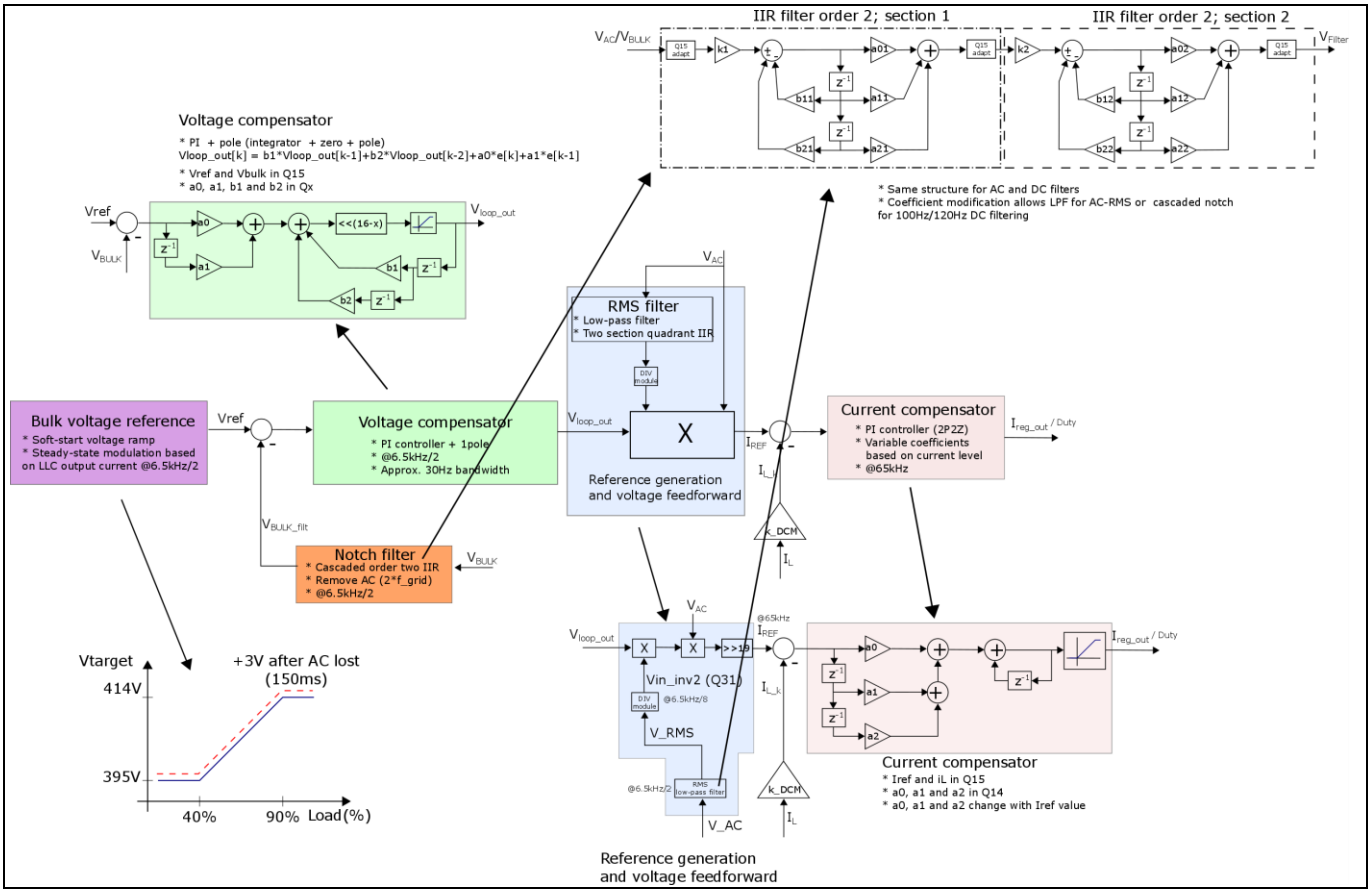


Figure 24 1600W PSU PFC control scheme

These SW blocks are presented in blue in Figure 25, together with the required HW peripherlas (red) for proper operation of the PFC stage. The used peripherals can be summarized as follows:

- Three CCU8 slices: two slices configured in compare mode to generate the PWM for the PFC switch and ADC trigger; one slice used in capture mode for conduction time adquisition in discontinuous conduction mode (DCM).
- Three CCU4 units used as fixed frequency interrupt trigger and reference generation for the analog comparators (peak limitation and DCM conduction time capture).
- Two analog comparators: one for peak current limitation using the CCU8 trap functionality and one for zero current detection during DCM operation.
- Division unit of the Math coprocessor: the use of this peripheral allows a reduction in the division computation up to 4 times in respect to the standard SW implementation.
- Four analog-to-digital conversion (ADC) channels with two different triggers for synchronized voltages and current sensing.
- AC input is used via a GPIO to obtain the input voltage polarity.
- One USIC channel is configured for UART operation to communicate with the LLC stage.

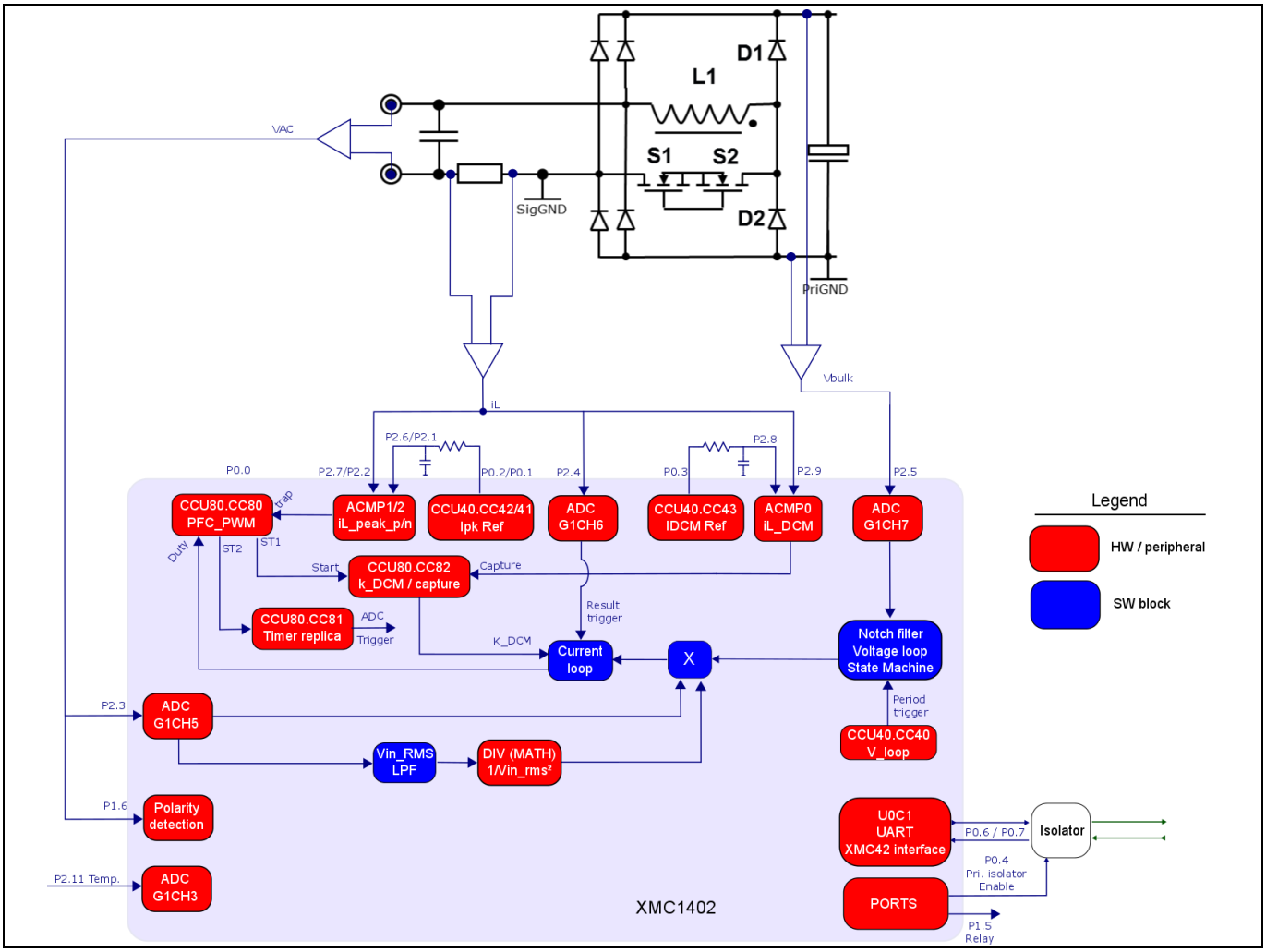


Figure 25 Peripherals and SW blocks used in the PFC of the 1600W server power supply

The CCU8 unit available in the XMC1402 microcontroller is a two channel capture-compare unit. The possibility of using these two channels independently, together with the versatilty of the ADC and the programmable signal conditioning between the timer and ADC modules, allows a synchronized and noise free sensing of the necessary voltages and currents for PFC operation.

Figure 26 shows the time diagram of the ADC sensing and interrupt service routine (ISR) trigger of the implemented current loop, which is executed every switching cycle (f_{sw} = 65kHz). Compare channel 1 (CR1) of the main timer (PFC PWM) carries the duty cycle information. However, compare channel 2 (CR2) is set to half of CR1 value to trigger the ADC queue [8]. Therefore, the inductor current is sensed in half of the on-time, which corresponds to the inductor current average value in CCM operation. The result event of the ADC is used to trigger the current control ISR, which ensures using the last adquired current value.

At the same time, a second timer (Timer replica) is synchronized with the main timer. The use of the replica allows synchronising as well the bulk voltage measurement. In this case, a second ADC group, e.g. the scan ADC[8], is triggered in the middle of the off-time, thus reducing the sensing noise.

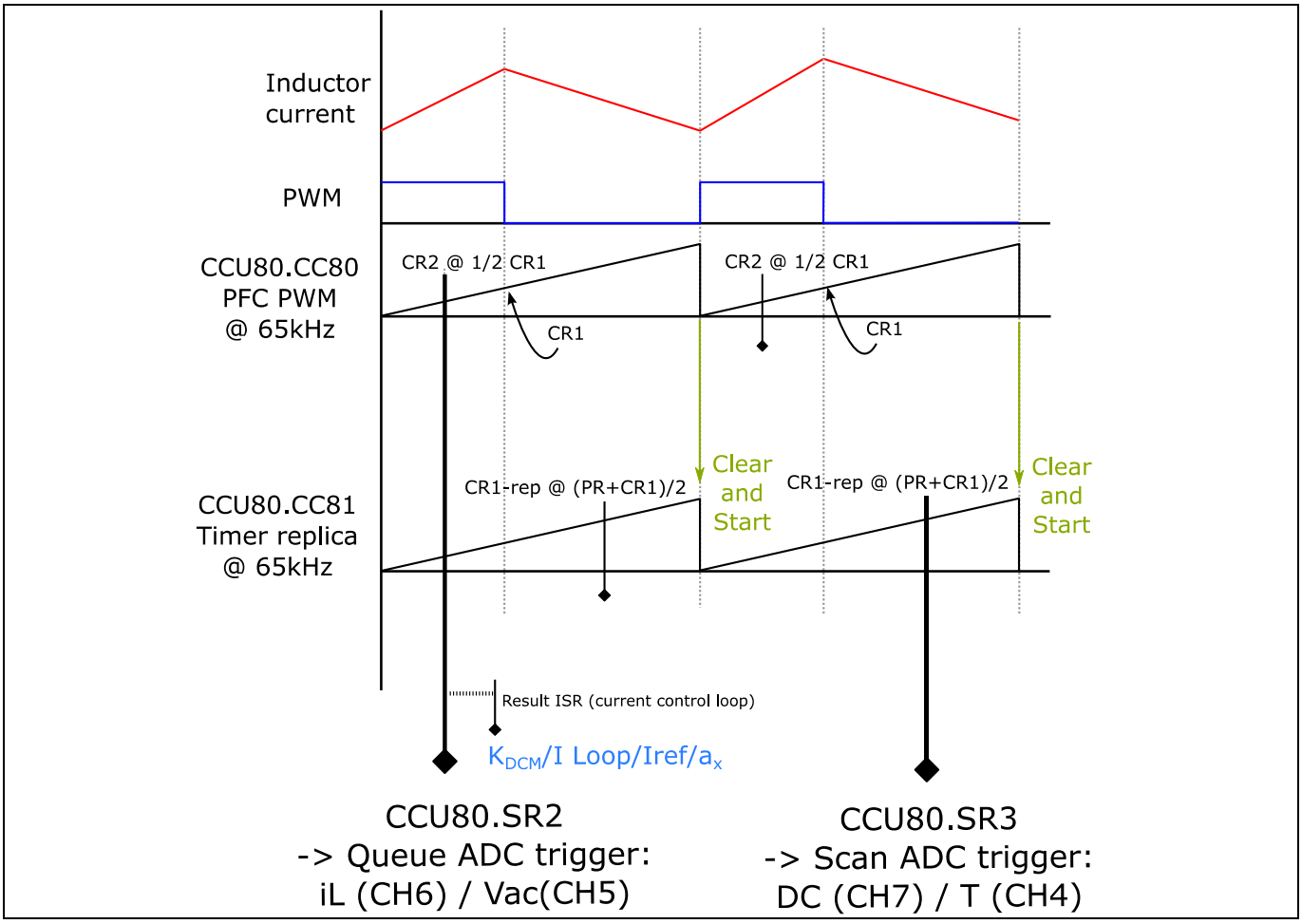


Figure 26 Timers and ADC synchronization in the implemented PFC control scheme.

The voltage loop, PFC state machine, low pass filter (LPF) of the input voltage and bulk voltage notch filter and monitoring are implemented in a second ISR triggered at a fixed frequency of 6.5kHz using a CCU4 slice. The scheduling of these functionalities is shown in Figure 27.

Both the AC filter (LPF of the AC voltage) and the notch fitler of the bulk voltage are two cascaded sections of second order IIR filters (see Figure 24).

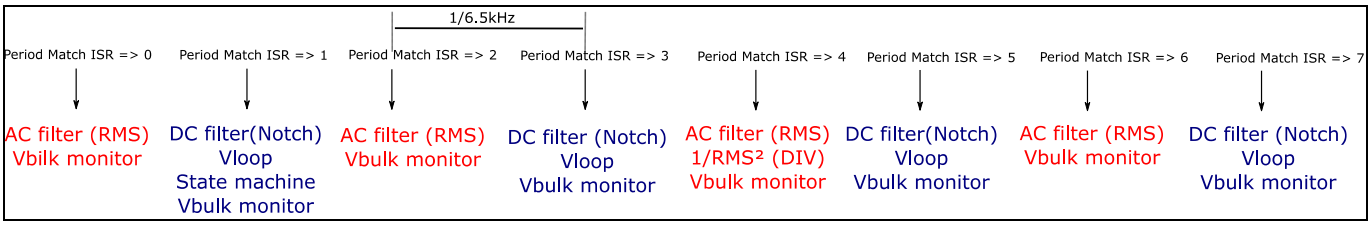


Figure 27 Time schedule of the voltage loop interrupt at 6.5kHz.

The state machine (Figure 28) ensures the correct behavior of the PFC system by controlling the start-up phase and monitoring the output and input voltage during operation. During startup the relay is closed before the boost converter starts switching, in order to bypass the NTC resistance which limits the inrush current. The relay is then open only in case the bulk voltage goes under a defined level, under which the PFC is restarted.

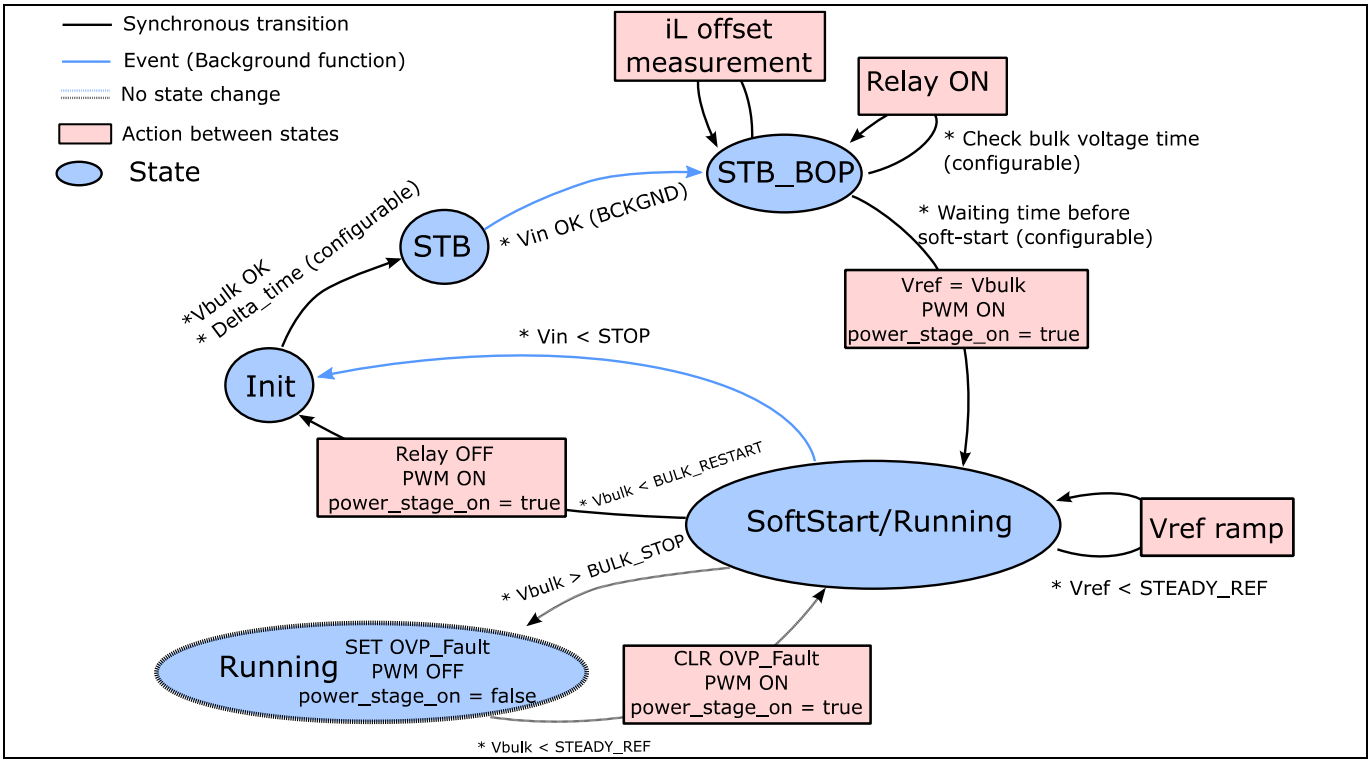


Figure 28 PFC state machine

3.1 Current loop interrupt

The selected controller for the current loop is a PID digital controller implemented with a 2P2Z difference equation as shown in the general control structure presented in Figure 24.

The current controller structure in the bridgeless PFC with bidirectional switch is the same than in the classic PFC of the 800W PSU presented in [1] and [2]. This structure allows facing different issues which rise during PFC operation: variable inductance due to saturable core, DCM operation at light load and filter interactions. The overall flow diagram of the current loop ISR is introduced in Figure 29.

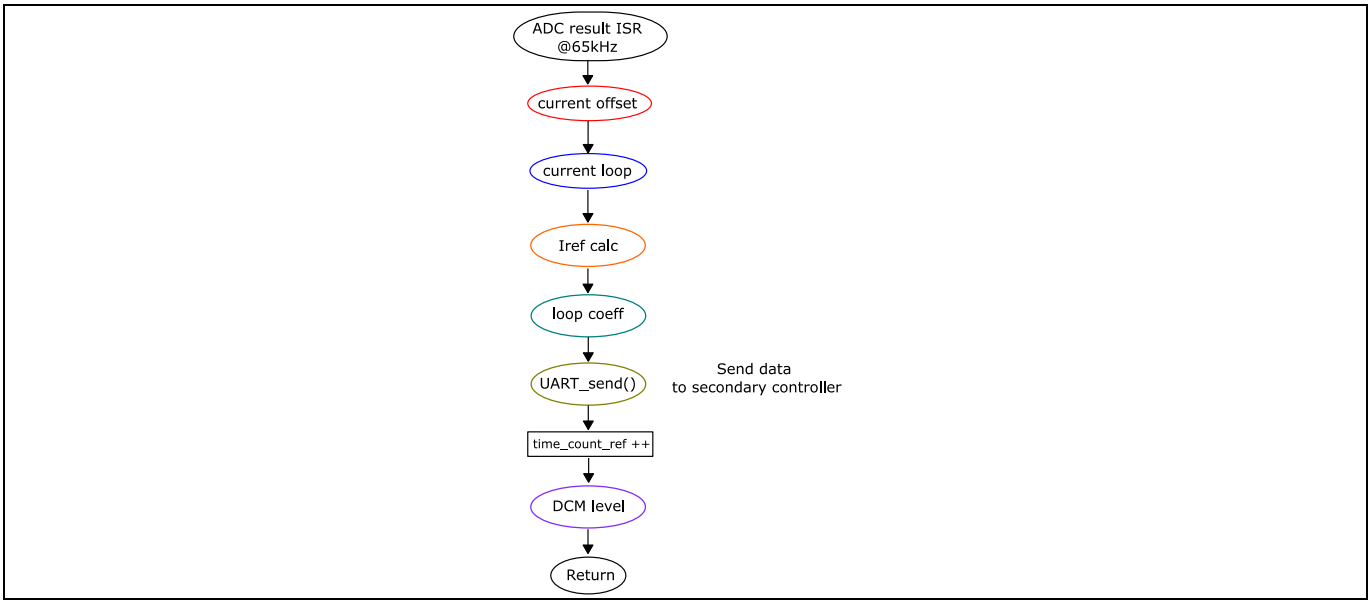


Figure 29 Simplified flow diagram of the implemented current loop in the PFC of the 1600W server PSU.

In the following paragraphs a more detail explanation of the implemented algorithms will be presented.

The current sense in the selected bridgeless topology is done with a shunt resistor in series with the PFC choke and therefore the measured current will be both positive and negative depending on the input voltage. The implemented current gain introduces a current offset which corresponds to half of the ADC voltage range (XMC1400 supply voltage). Since the measured AC voltage is rectified by the implemented sensing circuit, an offset removal and a SW rectification of the current measurement is required for proper PFC current loop operation, as depicted in Figure 30.

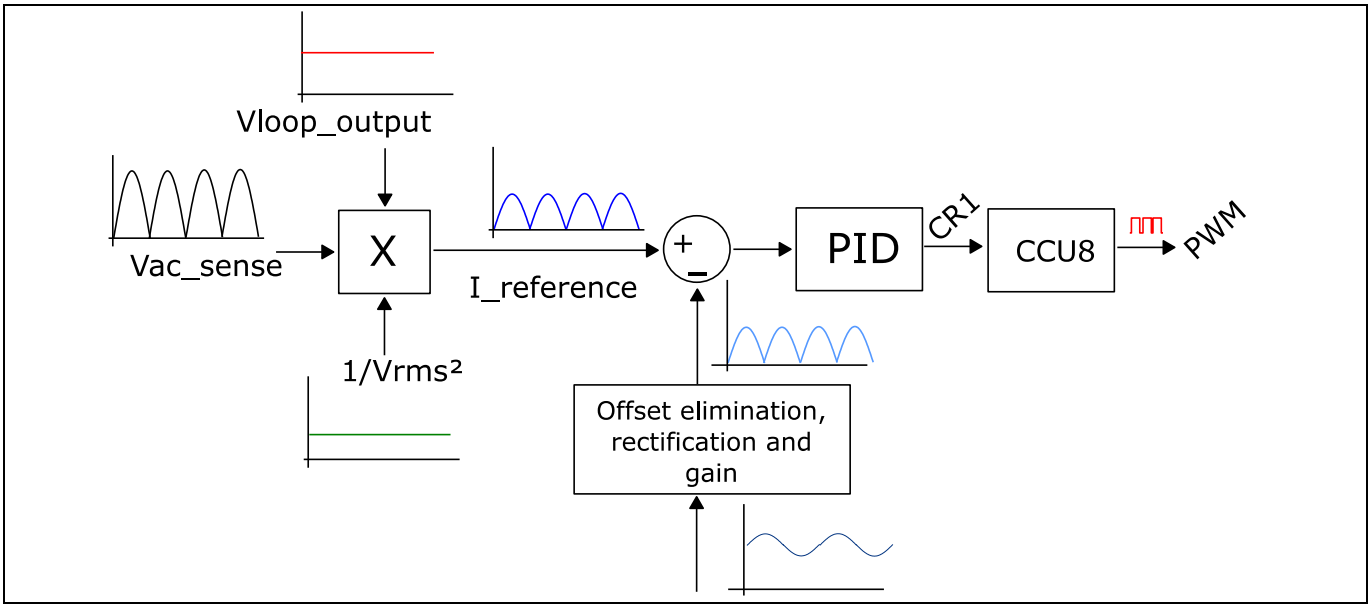


Figure 30 Current manipulation is required for current loop operation.

In order to increase the accuracy in the current sensing path, the actual current offset is measured before the PFC starts operation. Figure 31 shows the used algorithm for offset calculation, where iL_offset_en is set in the state machine.

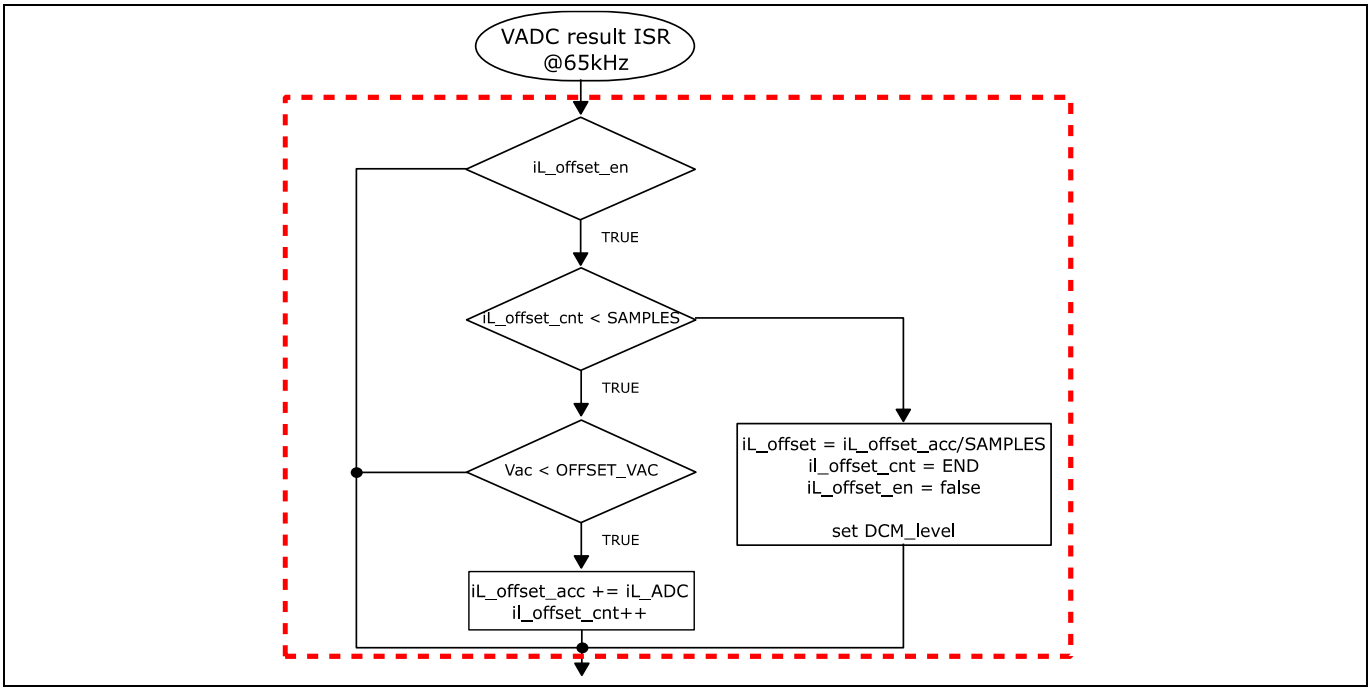


Figure 31 Offset measurement before start-up. Current offset in Figure 29

The calculated offset is used to calculate the inductor current to be used in the current loop equation as depicted in Figure 32. Prior to the loop calculation the current without offset is corrected if DCM is detected (kDCM) and rectified in case is negative.

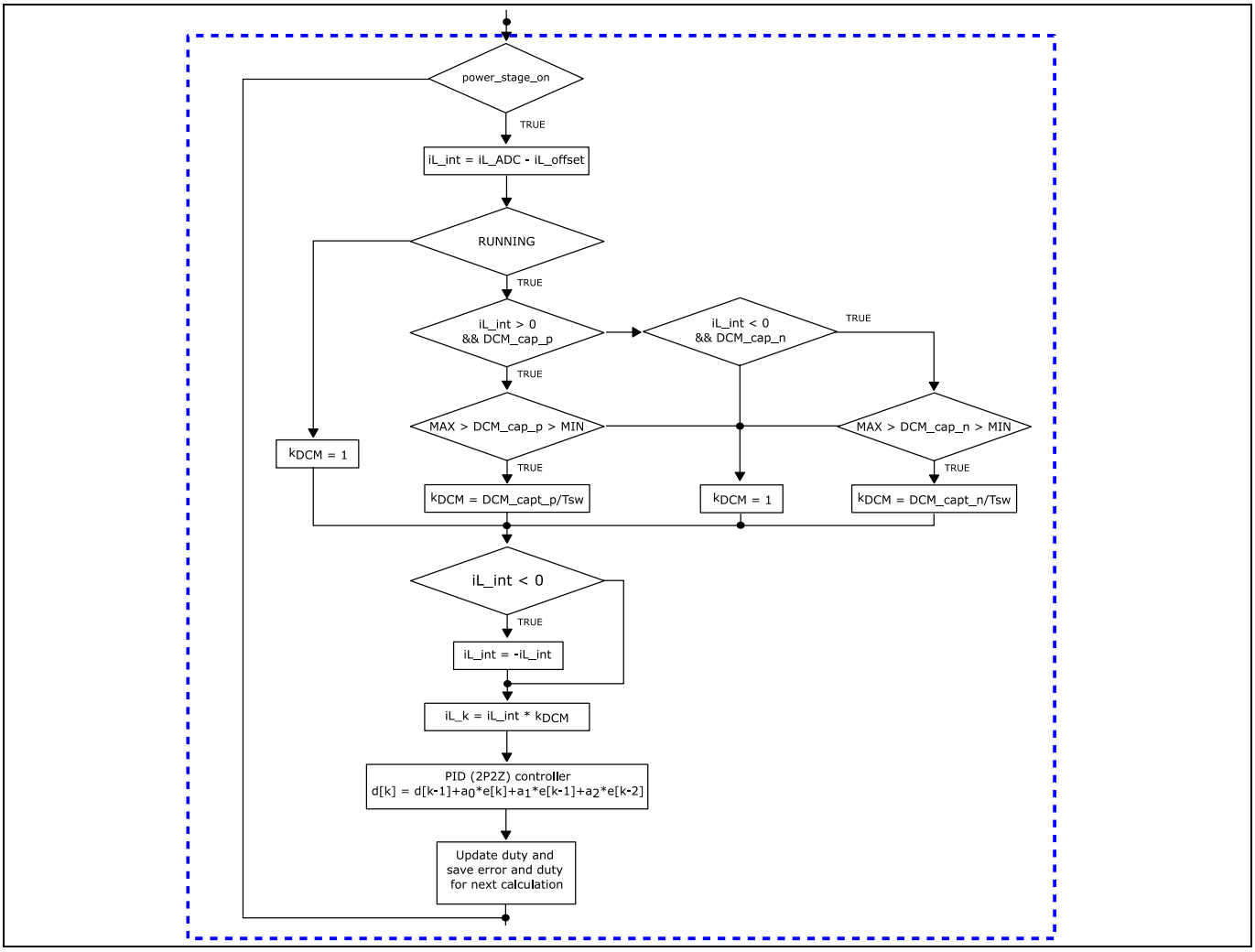


Figure 32 Current loop flow diagram including DCM factor calculation. Current loop in Figure 29

The kDCM calculation must be done for positive and negative half-cycle since, as already introduced, the sense current is positive and negative in respect to an introduced offset. The capture function of a CCU8 unit has been configured according to the comparator output edge as presented in Figure 33.

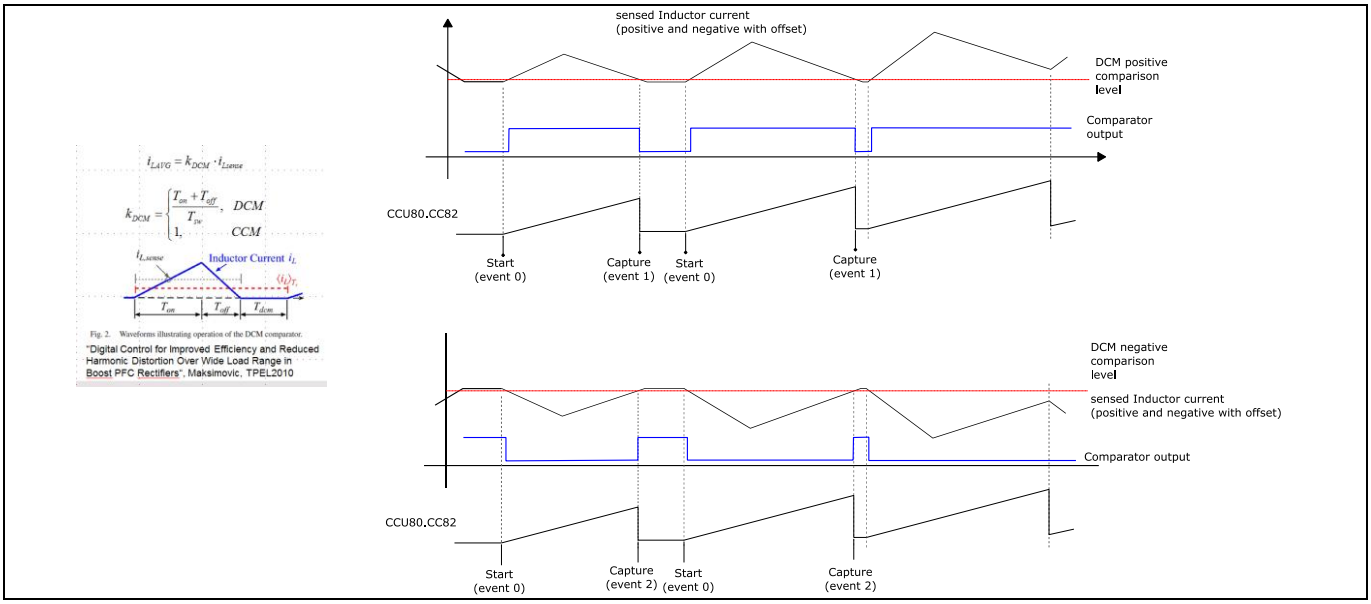


Figure 33 DCM conduction time capture for positive (top) and negative (bottom) input voltage.

The current reference used in the current loop is calculated in the previous ISR cycle using the AC voltage, the RMS value and the output of the voltage loop as shown in Figure 24. Some modifications to this value are introduced: the first one compensates the difference in AC voltage sensing for positive and negative haf-cycle, and the second one increases the reference in case the bulk voltage is under a defined value (voltage monitoring in Vloop ISR). Finally, the calculated reference is limited according to defined minimum and maximum values.

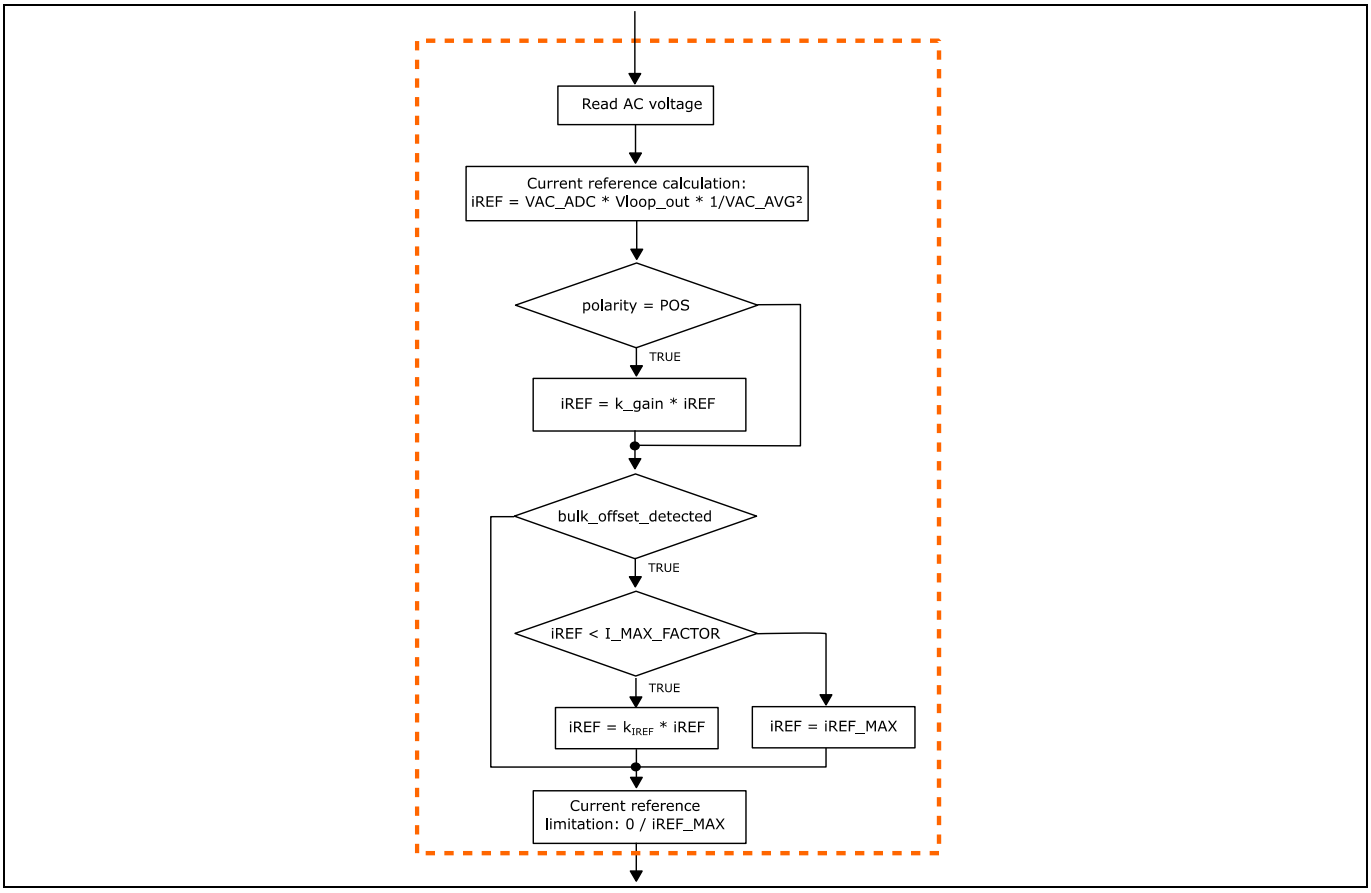


Figure 34 Current reference calculation. Iref calc in Figure 29.

The coefficients used in the currnet loop must be modified according to the current level to compensate the inductance degradation in the saturable choke [1] and [2]. The inductance has been coded in two linear regions (Figure 36).

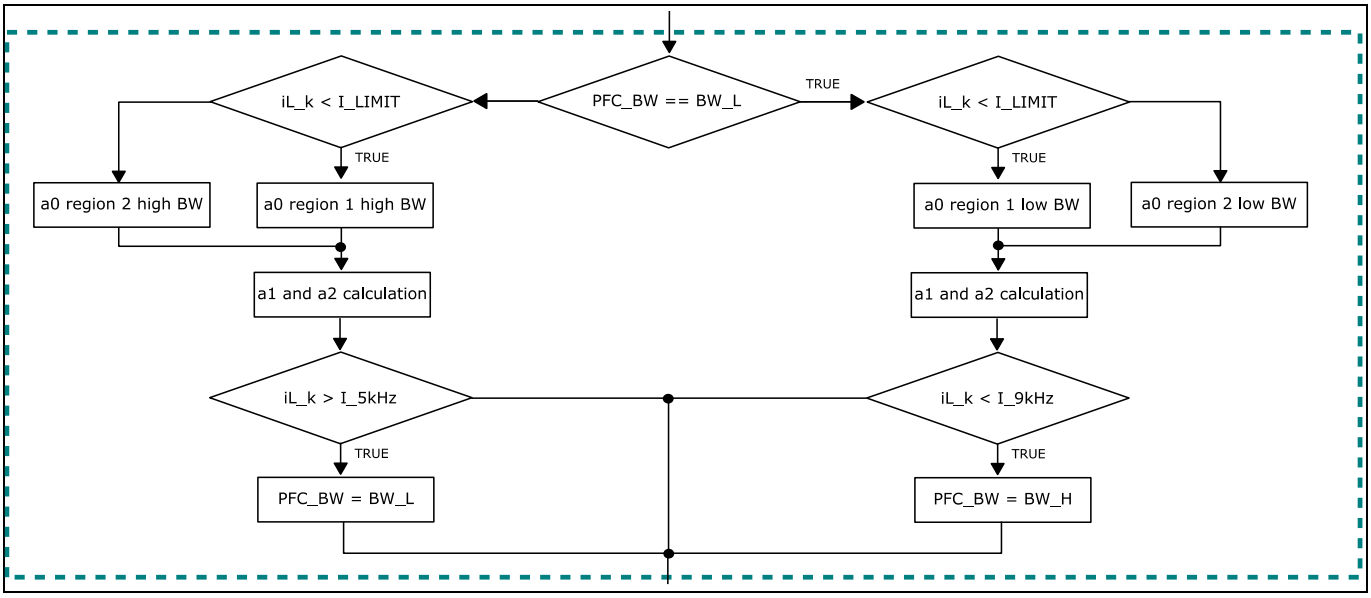


Figure 35 Loop coefficients calculation according to current level. Loop coef in Figure 29.

Figure 36-right shows the BW change implementation according to the sensed average current. A high BW is kept under 6A operation when there is no risk of filter interactions, in order to keep a good performance in terms of Power Factor and Total Harmonic Distrotion. However, when the current increases the BW is reduced to minimize the current oscillations due to filter interactions. A hysteresis is applied to avoid stability problems due to continuous BW modification.

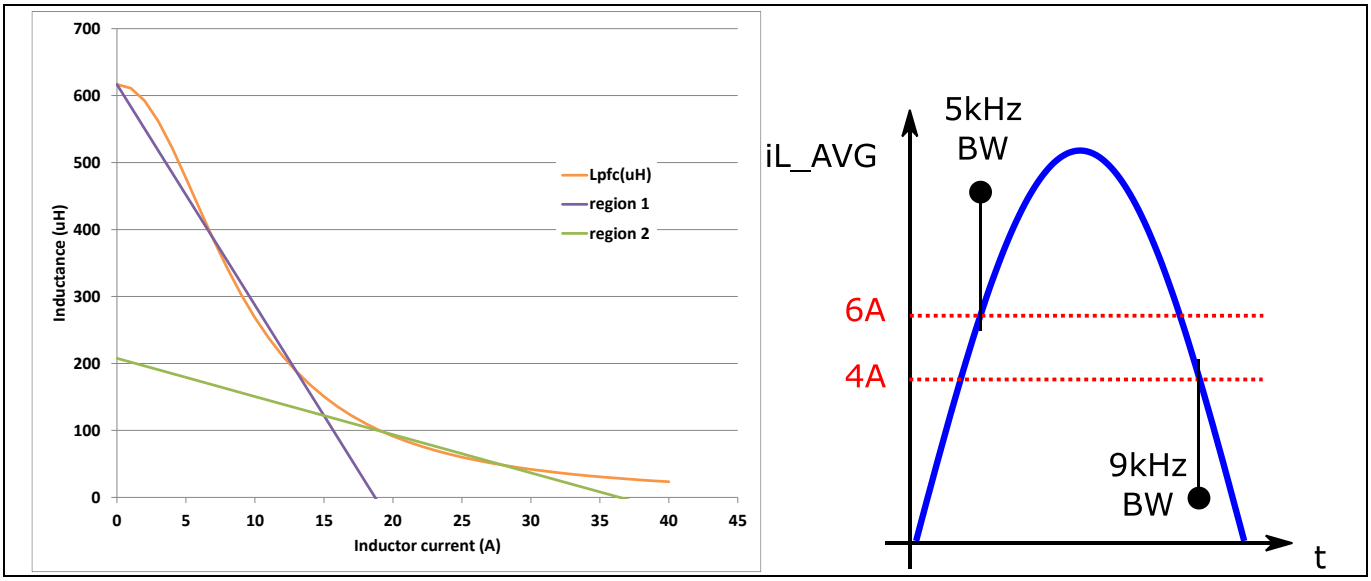


Figure 36 Linear regions to code the inductance variation (left) and BW change according to current level (right) to limit filter interations.

The last tasks in the current loop ISR are (Figure 37): sending voltage and temperature information to the LLC controller (via UART) and modify the DCM comparison level depending on the input voltage polarity, for propoer operation of the DCM detection shown in Figure 33.

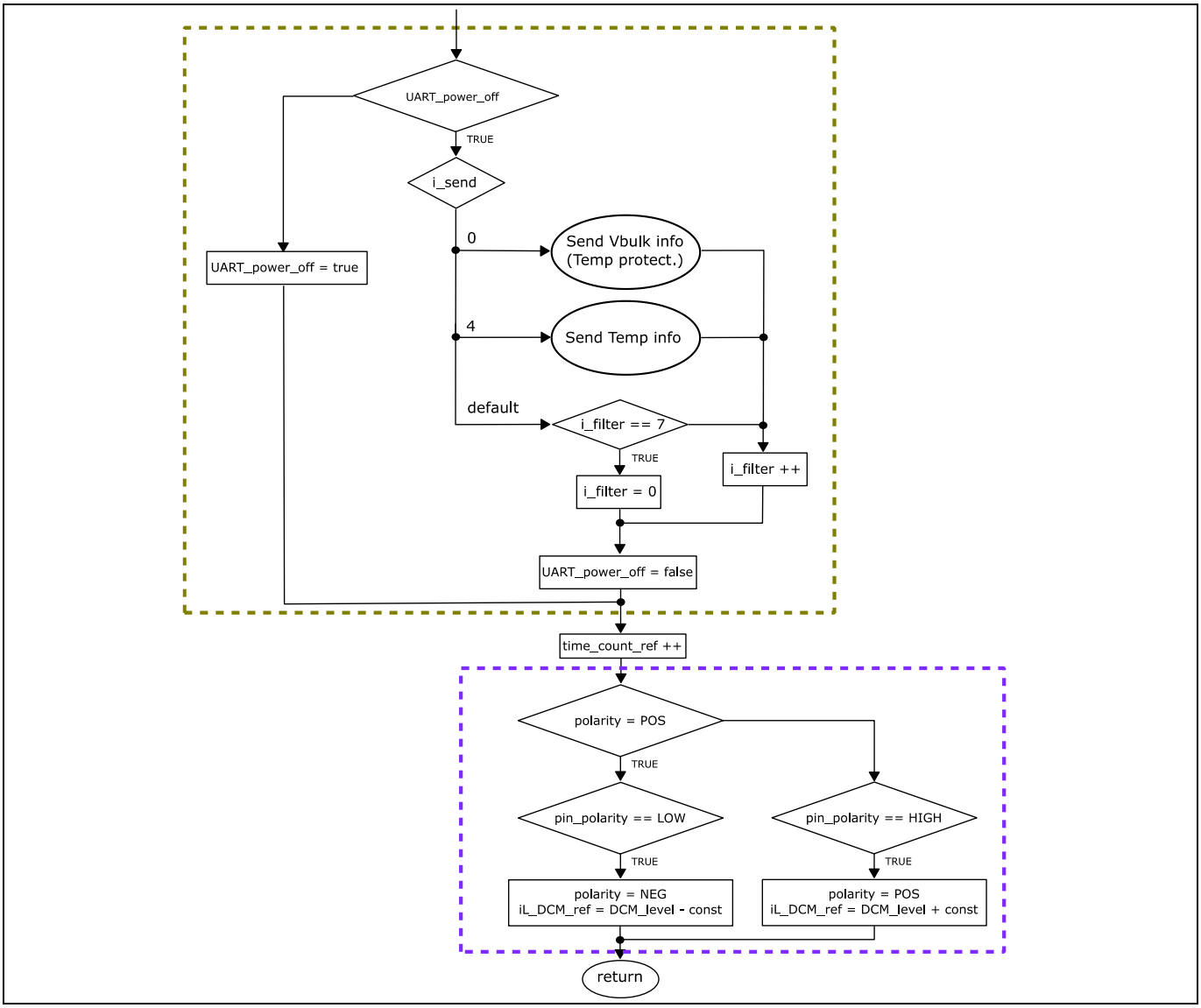


Figure 37 Sending information and modification of DCM detection level are the last tasks presented in Figure 29.

3.2 Voltage loop interrupt

As introduced in Figure 27, the voltage loop ISR is triggered at 6.5kHz using a CCU4 timer and a part from the loop calculation, voltage monitoring, RMS calculation, state machine and notch filter functionalities are implemented in the same ISR.

The notch filter (100Hz and 120Hz cascaded) and the low pass filter to calculate RMS value are implemented with a cascaded IIR filter structure as the one depitcted in Figure 24. The control design follows the same concept as presented in [1], [2] with a bandwidth close to 30Hz. The state machine has been presented already in Figure 28. In this section, more insight of the AC lost detection and bulk monitoring will be presented.

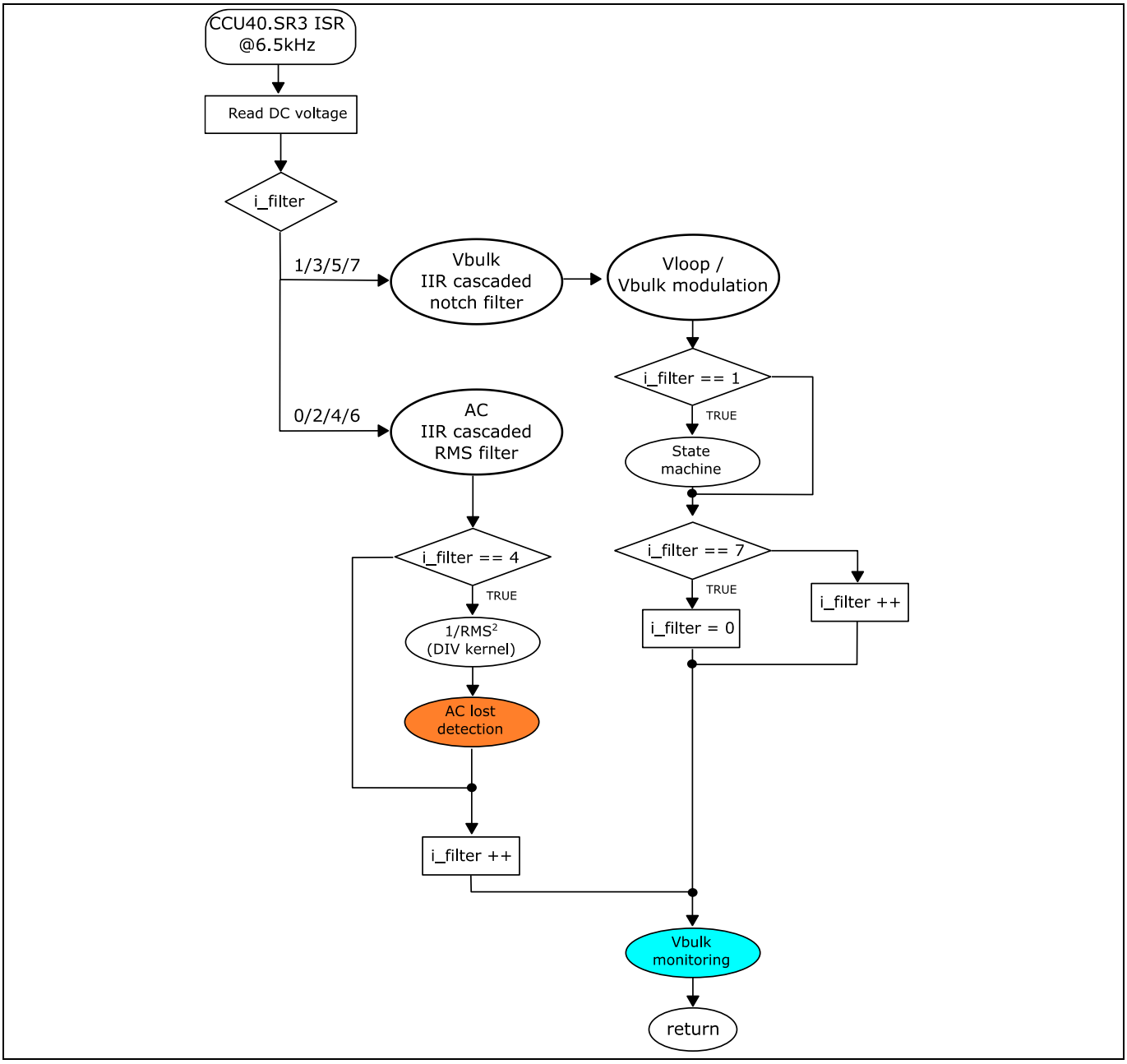


Figure 38 Overall flow diagram of the voltage loop ISR.

Three main situations are considered in the bulk voltage monitoring algorithm depicted in Figure 39. They are shown in Figure 40 and are: overshoot, undervoltage and voltage offset during AC line cycle abnormal conditions. This last one generates the flag used in the current loop to increase the current reference. In the case of overshoot, the PFC will stop switching until the voltage returns to the target voltage. If during operation, the bulk voltage decreases under a defined value (320V) the PFC stops operation and tries to restart a defined waiting time.

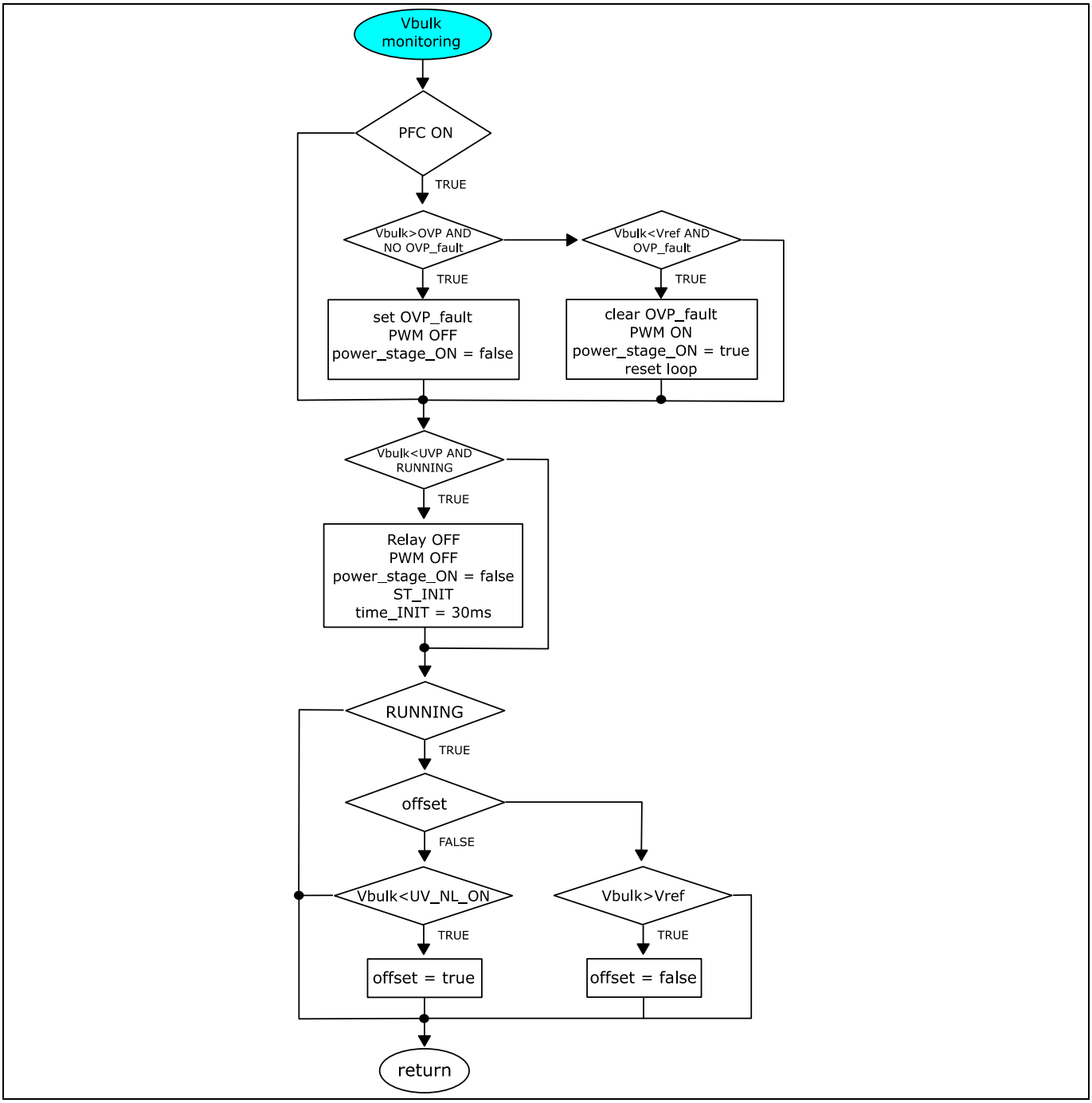


Figure 39 Bulk voltage monitoring flow diagram.

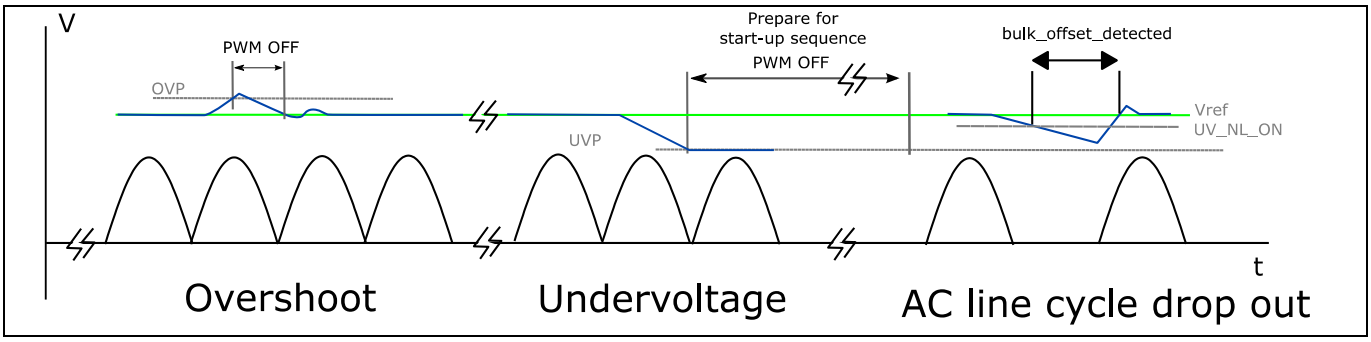


Figure 40 Bulk voltage monitoring situations.

The inverse of the RMS square value used in the current reference generation (line feedforward) is calculated using the divison kernel of the co-processor peripheral present in XMC1400 [8]. In the chosen implementation the co-processor is not blocking the XMC core and the calculation time is used for AC lost detection. As shown in Figure 41, if the AC voltage stays under a defined zero level (10V) for more than 3ms the acok signal is set false. On the contrary if the AC value goes over the peak value for 165Vrms, the acok signal is set true. This signal can be used for the LLC and to report to the outside system the lack of AC voltage. In addition, a timer is set to 150ms in which the bulk voltage reference is increased in order to facilitate the AC line cycle drop out recovery. The bulk voltage is modified in the “Vloop/Vbulk modulation” block in Figure 38. The voltage levels are shown in Figure 24.

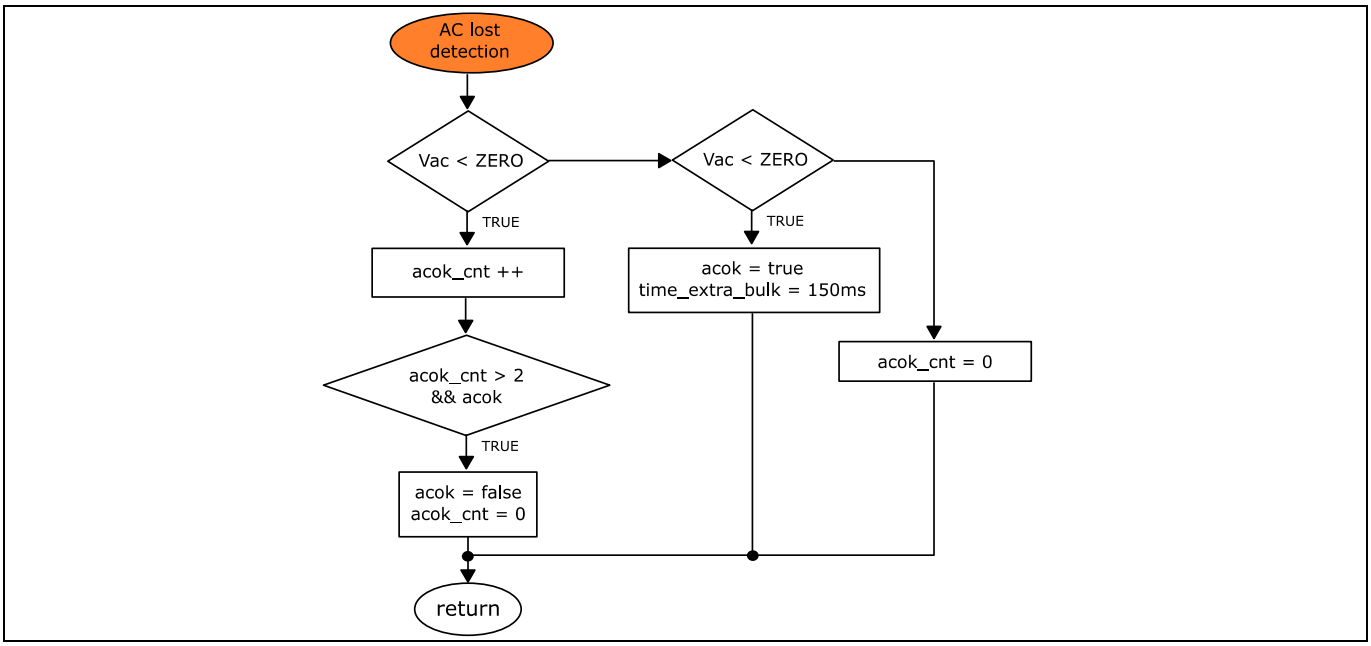


Figure 41 AC lost detection flow diagram.

3.3 Background processes

Three functions are run in the background, in the time where the interrupts are not executed. These functions are counting time for other processes in the PFC, monitoring of the input voltage and temperature sensing.

3.3.1 Time counter

Different variables are used to count required times for other functions in the current or voltage loop, or the start up process in the state machine. These variables are modified in two different groups which are updated at 1ms and 100ms base, based on the 65kHz count variable implemented in the current controller ISR.

3.3.2 Input voltage monitoring

This background process implements the brown-in/out function in the PFC control. It allows the PFC to start if the input voltage is over the minimum required (174Vrms) when the PFC is OFF.

In the case the PFC is ON, the PFC will turn off if the voltage goes under the minimum voltage. However, two timers are introduced to allow the system to comply with power line disturbance requirements as presented in Table 3.

The implemented flow diagram is presented in Figure 42.

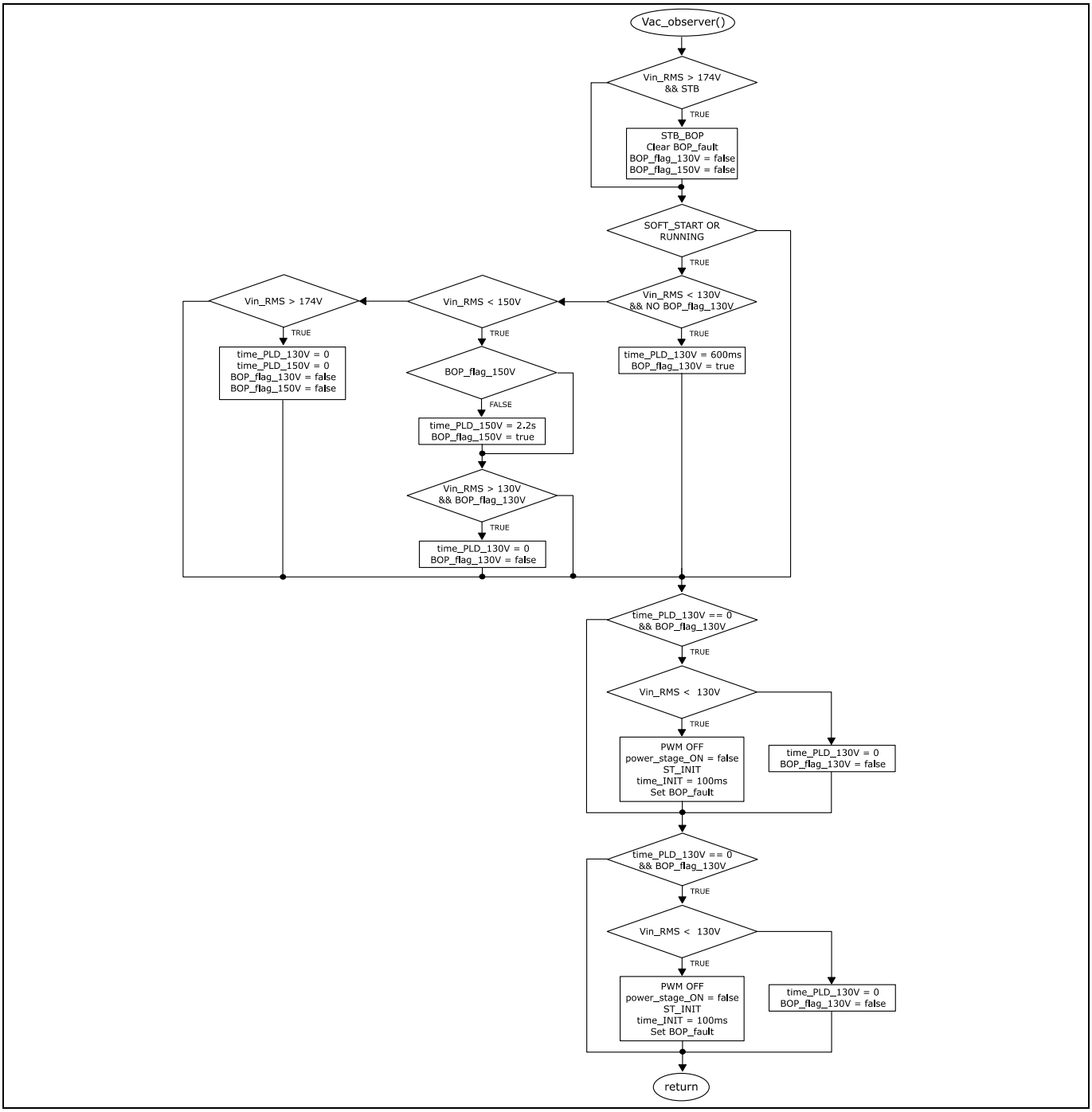


Figure 42 Input voltage observer background function flow diagram.

3.3.3 Temperature sensing

The fan control in the EVAL_1K6W_PSU_G7_DD board is done in the secondary stage microcontroller (XMC4200) by a PWM control. The temperature sensed in the PFC (XMC1400) is sent to the secondary side controller and used as input for the fan control.

Temperature adquisiton is done in a background process in the PFC controller structure. Two temperatures are sensed: the heatsink temperature via a NTC connected there and the internal chip temperature of XMC1402 (DTS/TSE [8]), which could be considered as ambient temperature during post-processing.

In both cases (NTC and TSE) the measurement is scaled to Celsius degrees and a linear approximation of the obtained ADC and TSE measurements is implemented. These two temperatures are reported to the secondary side controller as a single 16 bit value (Figure 37).

4 LLC control implementation

The DC-DC stage in the EVAL_1K6W_PSU_G7_DD board is a half-bridge LLC which has been design following the same concept than in EVAL_800W_PSU_4P_C7 and EVAL_800W_PSU_3P_P7 boards. The resonant frequency of the resonant tank is 160kHz.

The XMC4200 peripherals used in the LLC control implementation are shown in Figure 43, as well as the SW blocks, which correspong to interrupts.

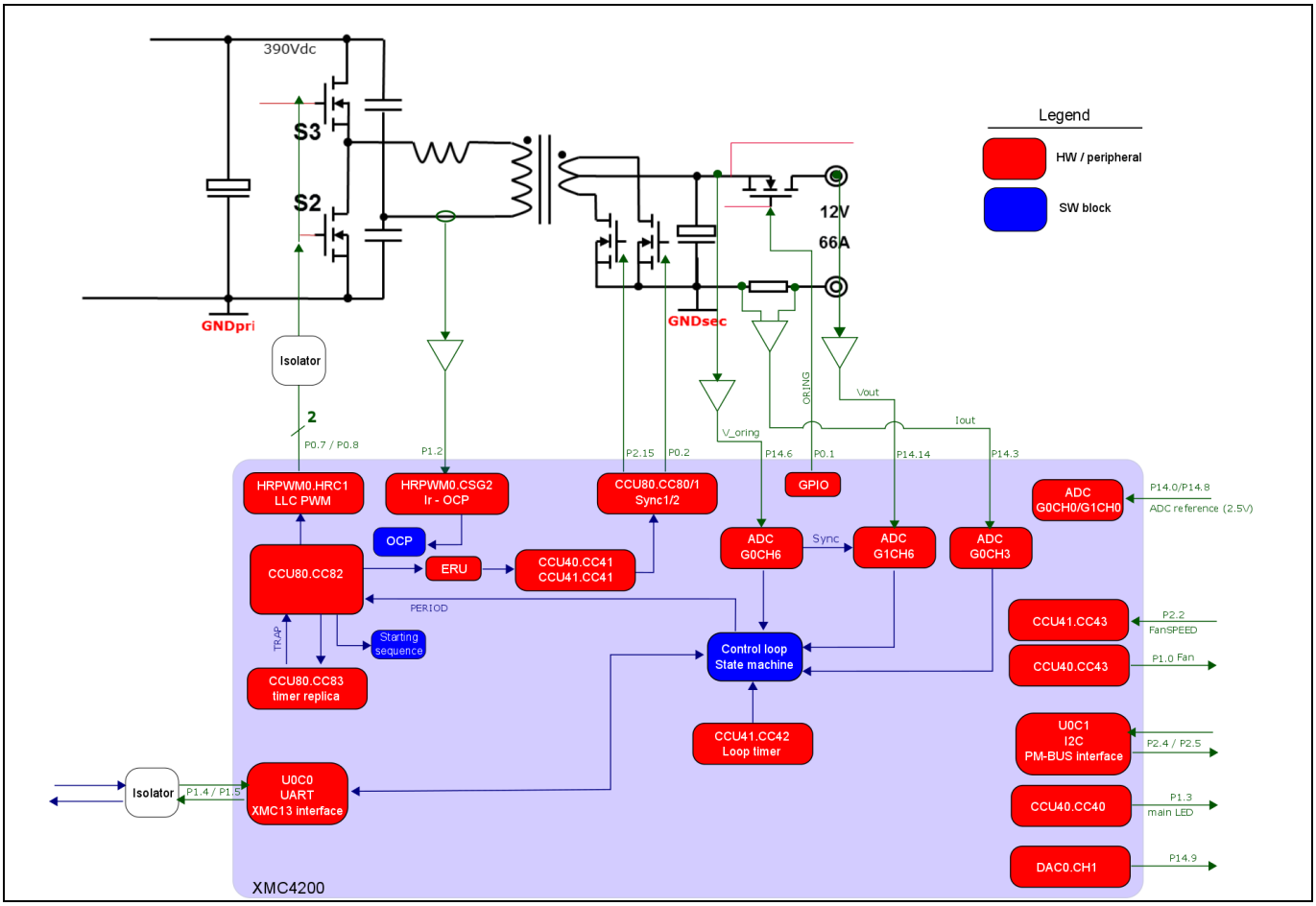


Figure 43 Peripherals and SW blocks in the 1600W PSU LLC control implementation.

Timer replica is used for trap function with synchronized exit (Figure 44). This allows synchronized turn off and on in situations such as burst mode, which implies a safe operation of the converter since the PWM period is always completed. The high resolution PWM (HRPWM) is used for synchronous modification of the dead time during operation.

The required timing for the synchronous rectification (SR1/2) switches in regards to the half-bridge operation is different if the LLC converter operates in under- or above-resonance conditions [9]. Despite the SW considers this timing, abrupt switching frequency changes might happen in case of dynamic situations, i.e. load jumps, which might lead to timing mismatch and device stress.

A HW configuration has been implemented taking advantage of the XMC4200 peripherals flexibility and connectivity, in order to avoid SR cross conduction or timing mismatch between primary and secondary driving signals in these conditions. The connection of the required timers is shown in Figure 44.

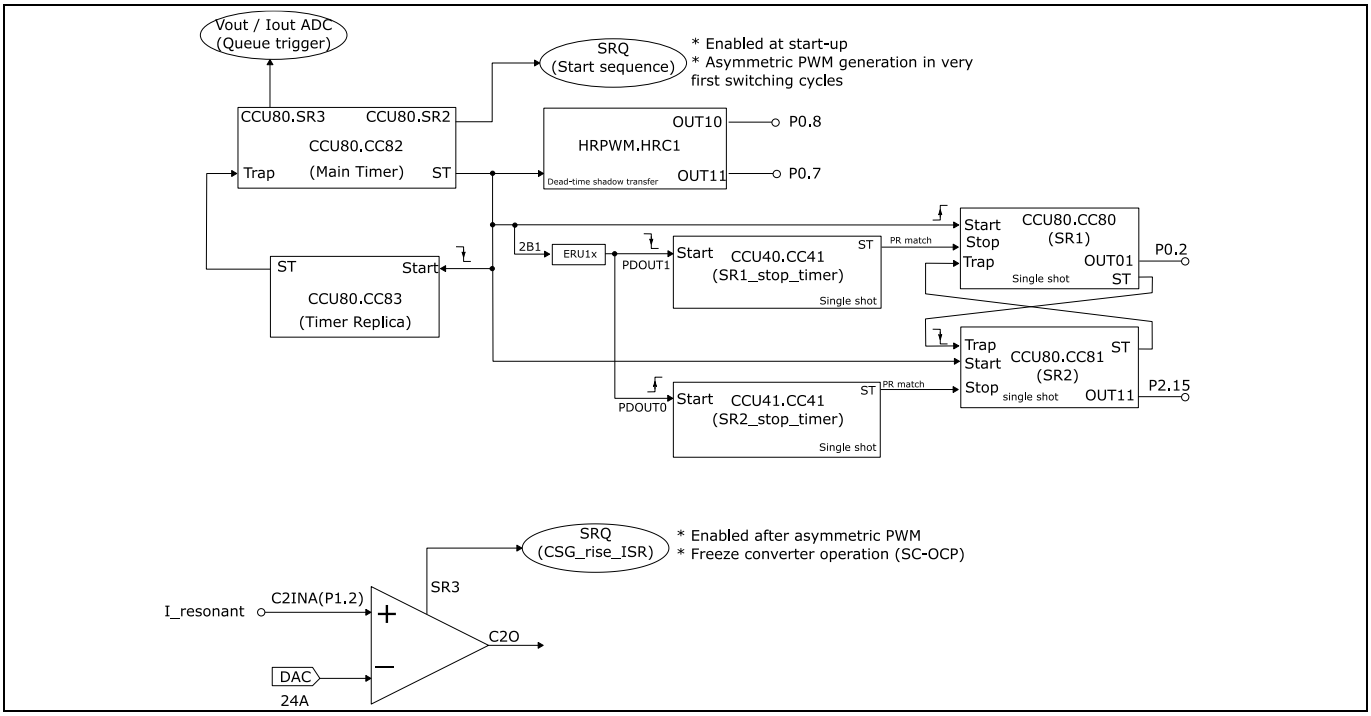


Figure 44 LLC timer configuration for the 1600W PSU with Infineon semiconductors.

An example of SR timing for above-resonance operation is shown in Figure 45. The single-shot CCU8 unit generating the SR1 PWM starts with the main timer period and the positive edge is delayed by SW. The negative edge, which ends SR1 pulse is either achieved by the programmed SW value (OFF delay) or a programmed timer to avoid SR crossconduction in transients (stop timer). The other Sync. Rect. signal is delayed 180 degrees in respect to the presented one. Furthermore, the SR1/2 signals trap each other, to further avoid SR missbehaviour.

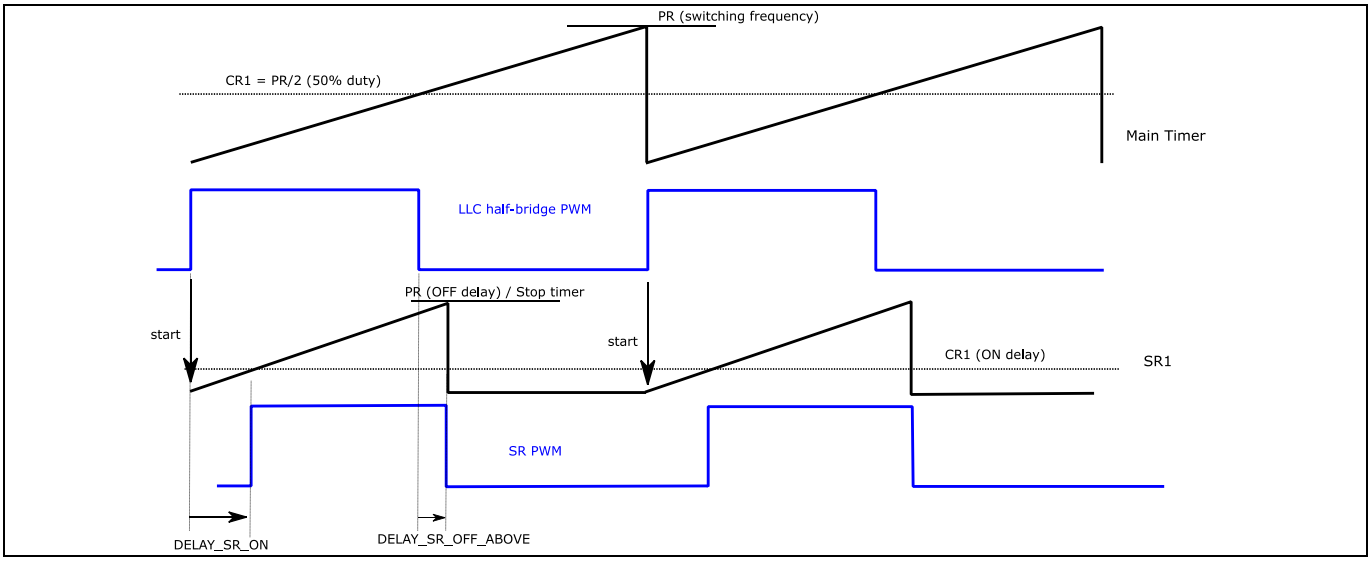


Figure 45 SR generation from main timer in above resonant operation.

As shown in Figure 43, three interrupt nodes are configured in the LLC control:

- Starting sequence: this interrupt is active in the first swicthing cycles only. It is triggered by the main PWM (LLC half bridge pulse pattern generation). In this interrupt the duty cycle and frequency of the PWM is

changed in order to generate a current in the resonant tank that avoids hard commutation in the first PWM pulses. This pattern is applied after a long time with the low side switch on, in order to charge the bootstrap capacitance (see state machine section for more details)

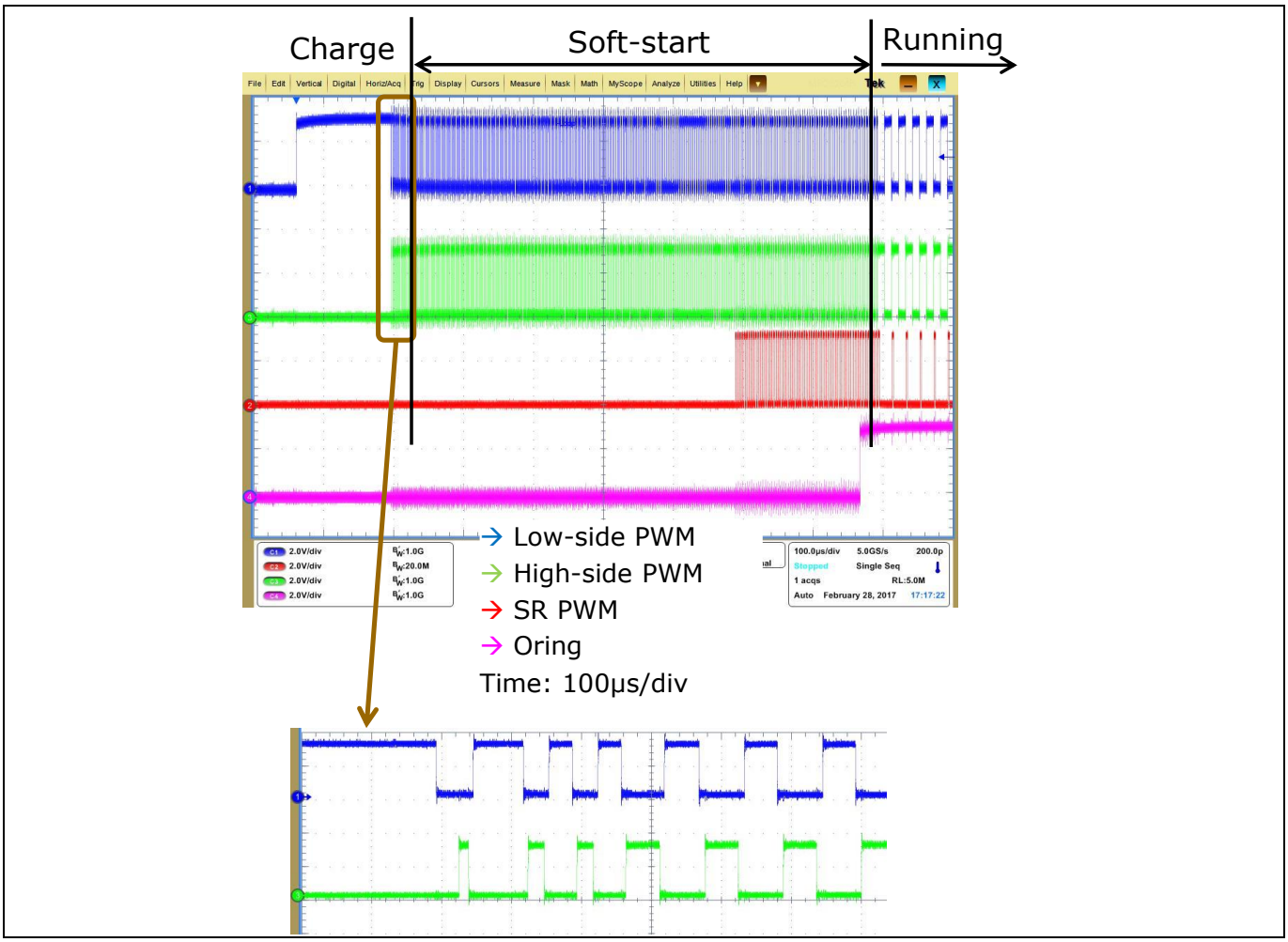


Figure 46 Asymmetric PWM operation in the very first switching cycles (bottom) during the start-up procedure (top).

- OCP: this interrupt is active after the starting sequence is done. It is associated to the output of the resonant tank current comparator. If this current reaches a predefined current threshold (56A) the comparator output transition triggers the interrupt and the converter operation is freezed. This guarantees a save turn off of the converter in high current situations such as short-circuit.
- Loop ISR: it is the main interrupt where all the control actions are taken. It is triggered at a fixed period (12.5µs) by a CCU4 unit. Figure 47 depicts the overall flow diagram of the control ISR. In the next sections, the different implemented functions will be explained in more detail.

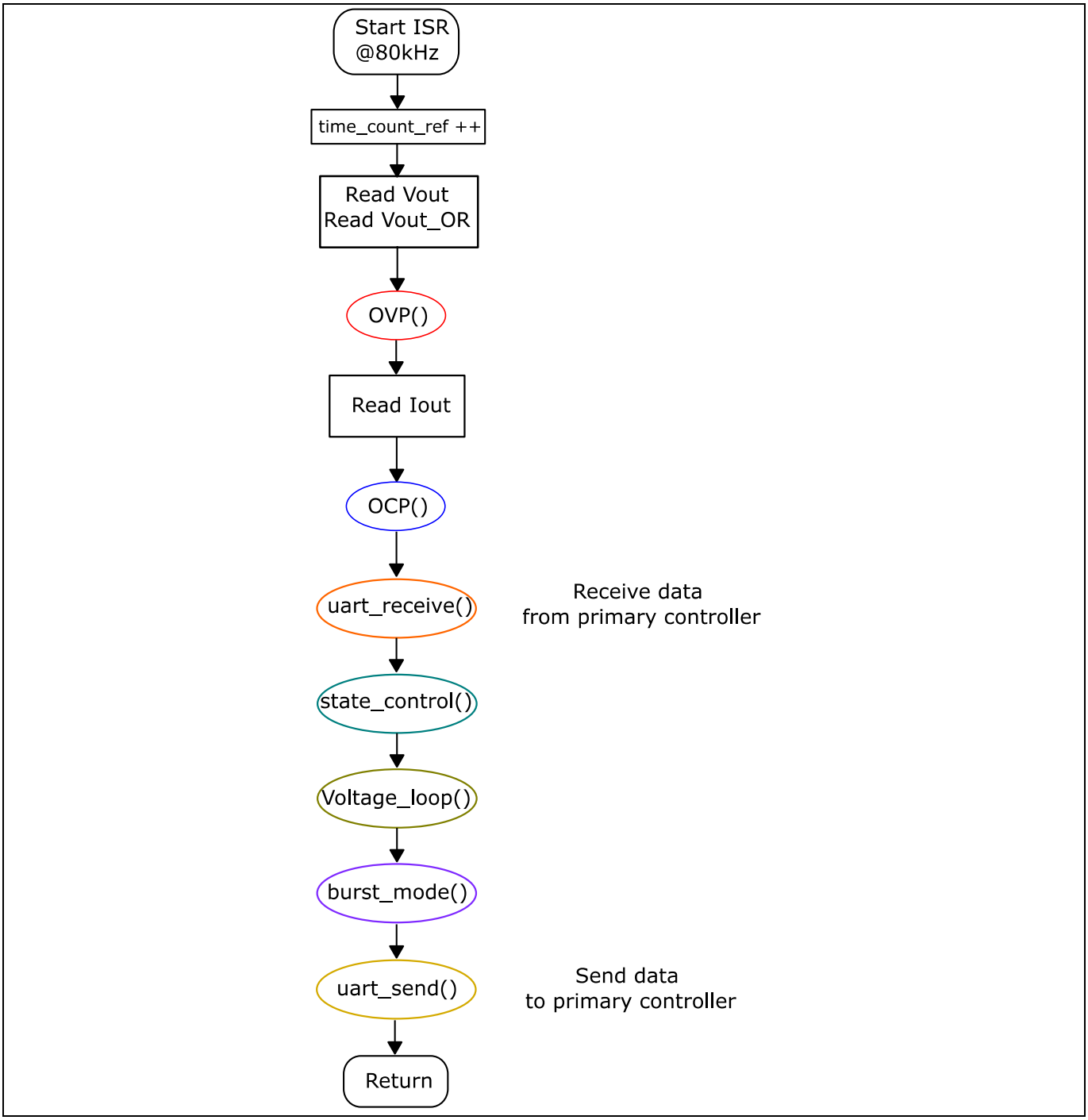


Figure 47 LLC control interrupt overall flow diagram.

LLC is a resonant converter which is controlled by frequency modulation and the control loop is evaluated at a fixed frequency as presented above. In order to get a proper voltages and currents sensing, the ADC trigger is associated to the PWM generation (switching frequency) while the information is used in the loop ISR as shown in Figure 48. This time mismatch might create control issues and it is taken into account in the controller design. Vout and Voring in Figure 48 are measured at the same time using the available channel synchronization in the VADC peripheral of XMC4000 family [10].

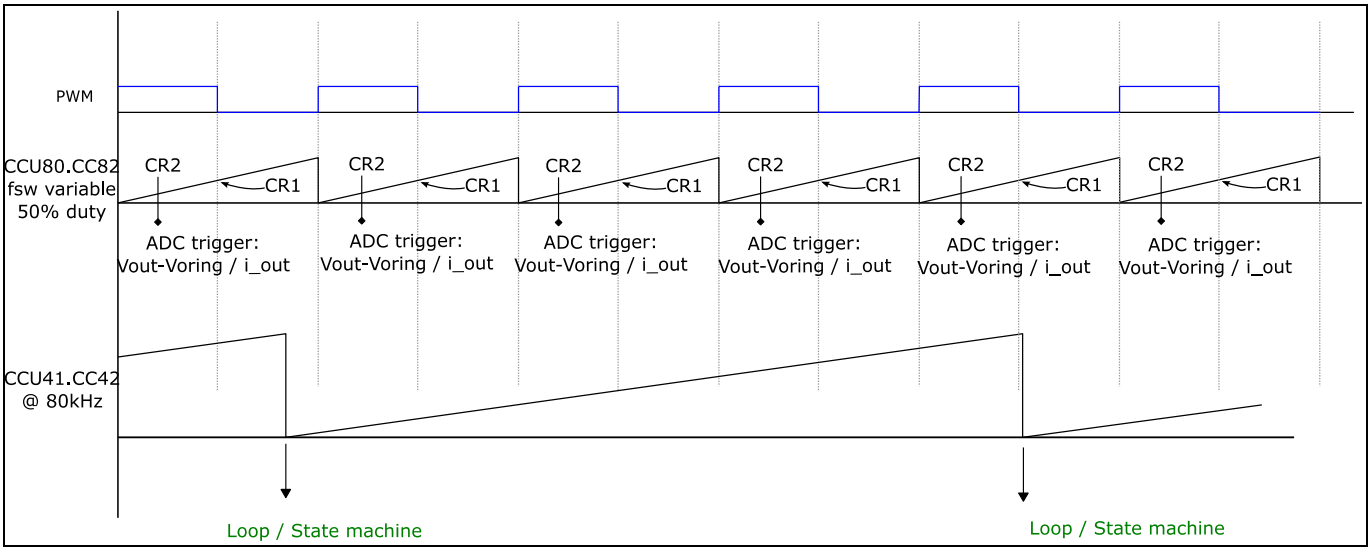


Figure 48 Time scheduling of the LLC control ISR and the Vout and Iout sensing for a given switching frequency.

4.1 Overvoltage and overcurrent protections

Both output overvoltage and overcurrent protection are SW protections, based on the ADC measurements. As introduced above a faster protection based on the resonant current comparison, has been introduced.

Overvoltage protection (Figure 49) is active when the converter starts switching and latches the operation if the output voltage reaches a defined threshold (14V) few samples in a row. The fault is cleared in the state machine if the bulk voltage decreases under a defined limit and the converter can restart.

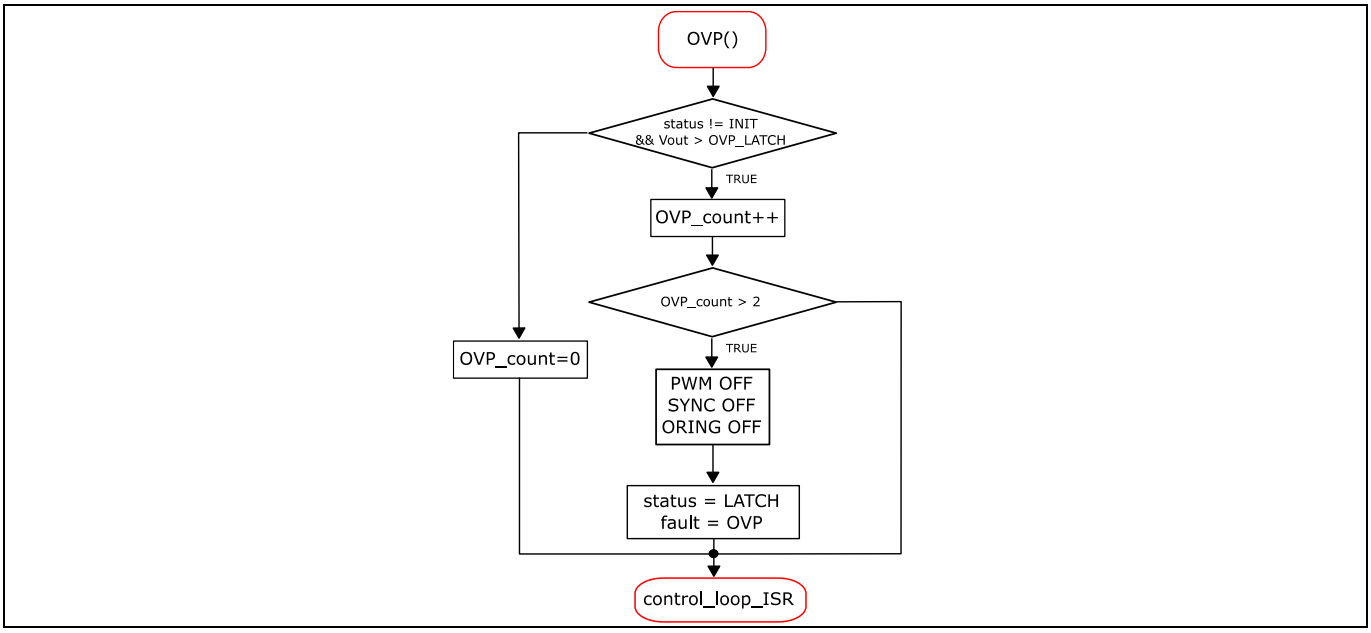


Figure 49 Overvoltage protection (OVP) flow diagram.

In the case of the overcurrent protection, the protection is latching as well until the bulk voltage is reduced under the same level than introduced before. In this case the protection is enabled at the beginning of the soft-

start. Its flow diagram is presented in Figure 50. Three different current levels with three different times (Figure 51) are defined in this protection, which allows the unit to provide extra power for a certain time.

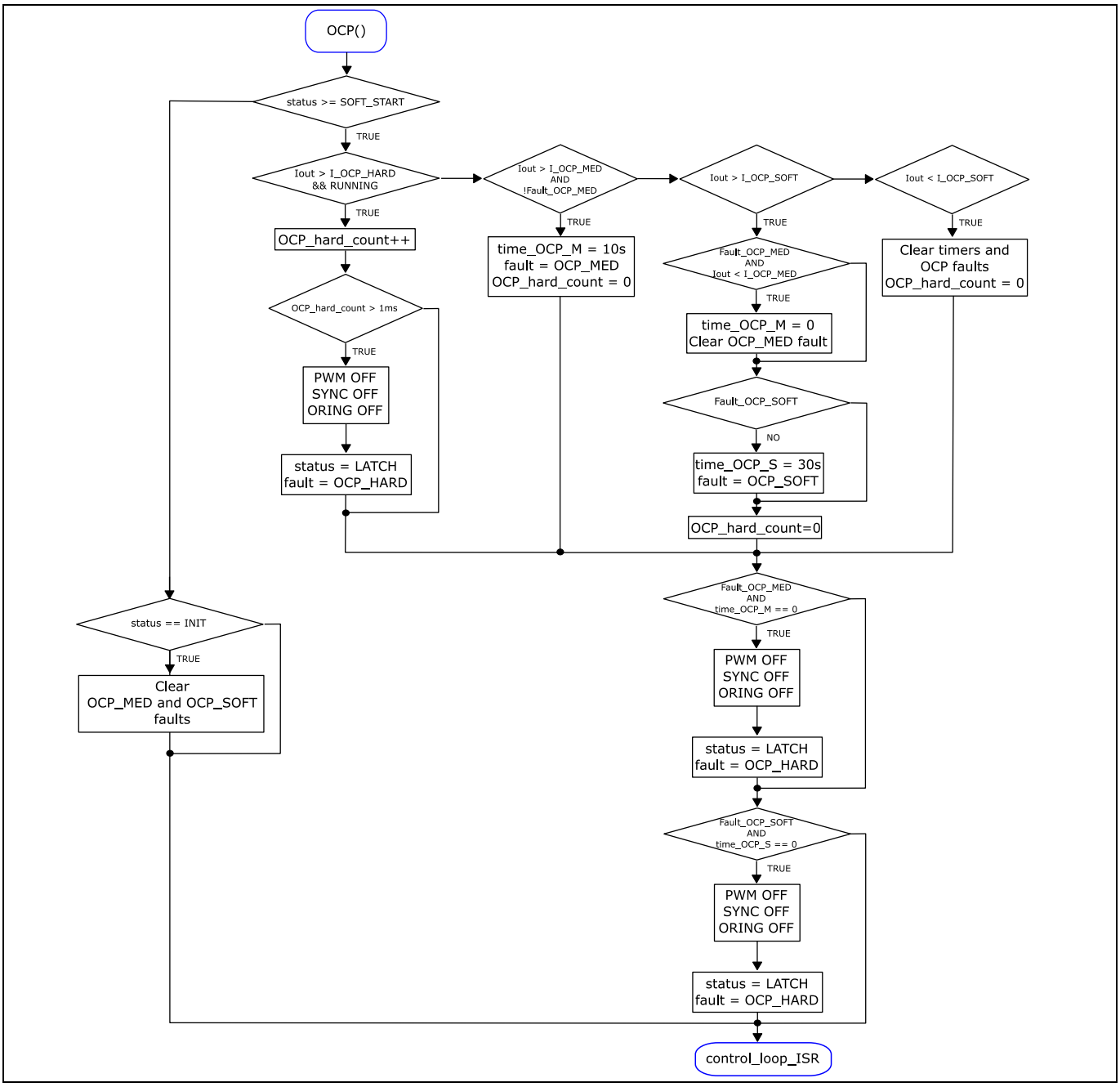


Figure 50 Overcurrent protection (OCP) flow diagram.

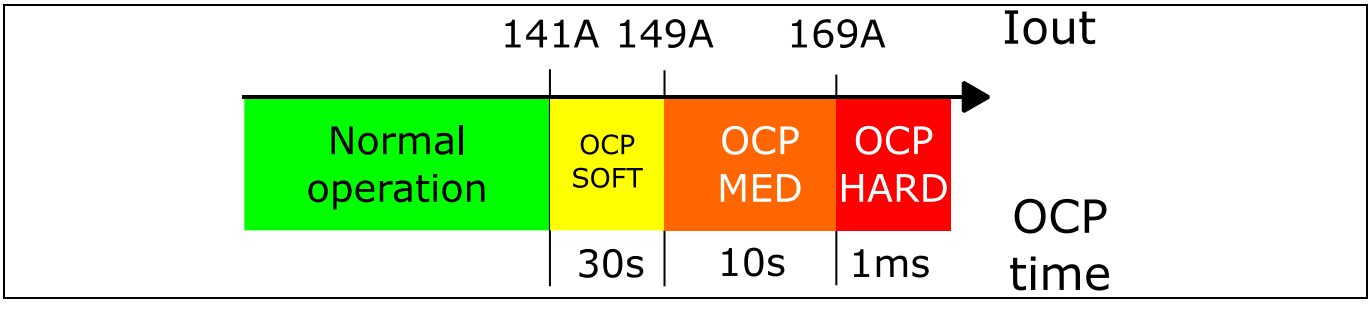


Figure 51 Timing and current levels implemented in the OCP.

4.2 Data transmission from/to primary controller

For the proper operation of the EVAL_1K6W_PSU_G7_DD server power supply, a communication between primary side (XMC1402) and secondary side (XMC4200) controllers is required. In the LLC this communication is managed in the main interrupt without requiring any dedicated ISR.

Two variables are received from the primary side: the bulk voltage information and the heatsink temperature (Figure 52). The second one is used in the background for fan control. The bulk voltage is used for the state machine. Parity bit error is used to ensure consistent bulk voltage data reception.

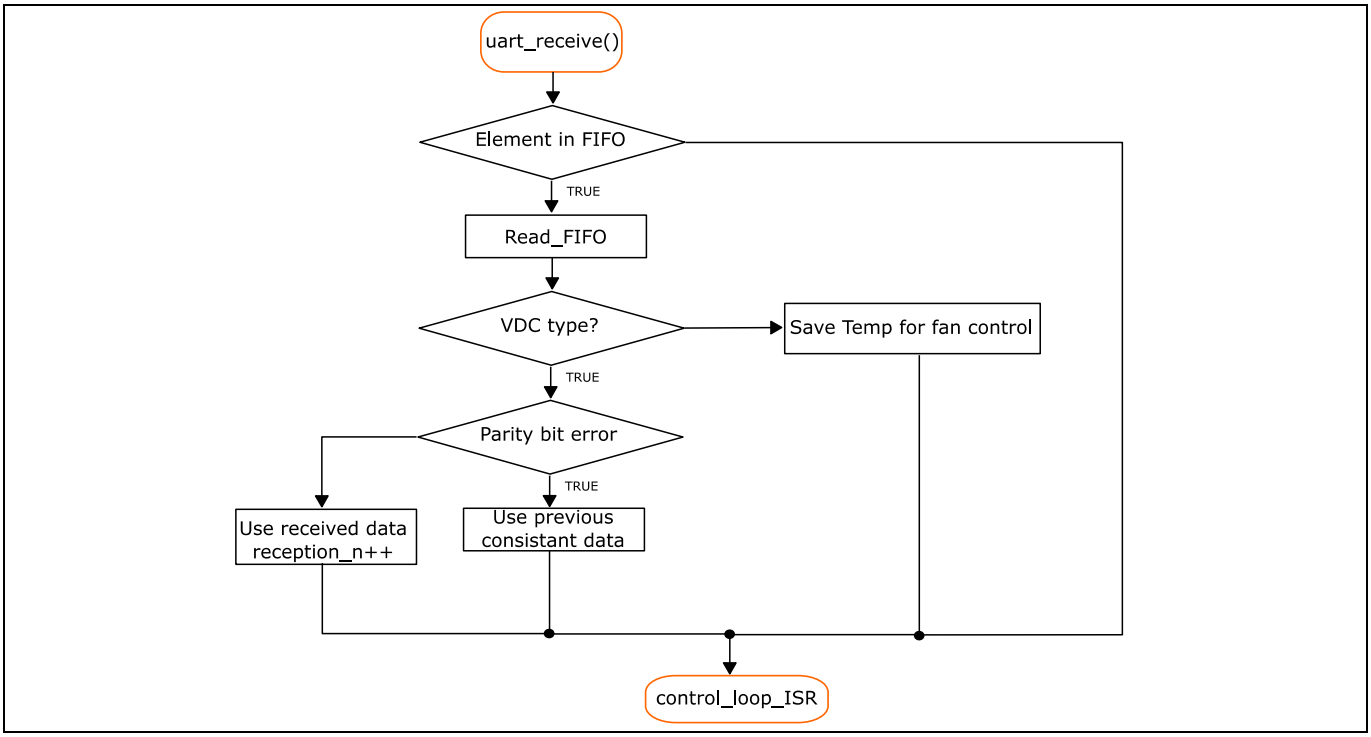


Figure 52 Bulk voltage and temperature reception procedure.

In the case of the information sent to primary side (Figure 53), the output current is sent to modify the bulk voltage according to the load as explained in the PFC section.

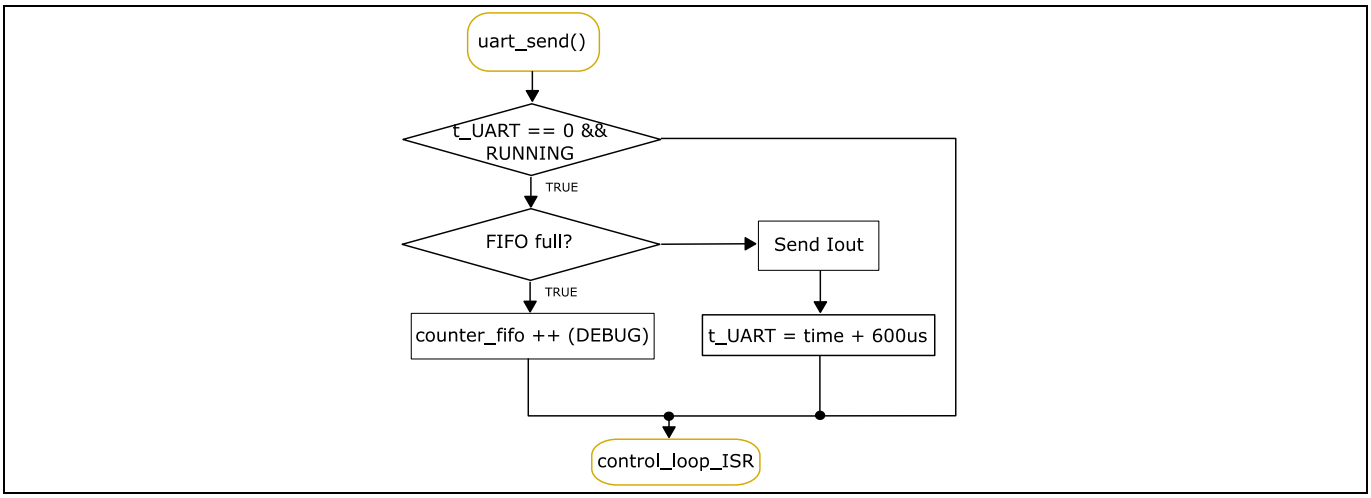


Figure 53 Output current is sent to primary controller.

4.3 State machine

The start-up and turnin on/off situations, such as burst or faults, are controlled in the state_control() function of Figure 47. The resultant state machine is presented in Figure 54.

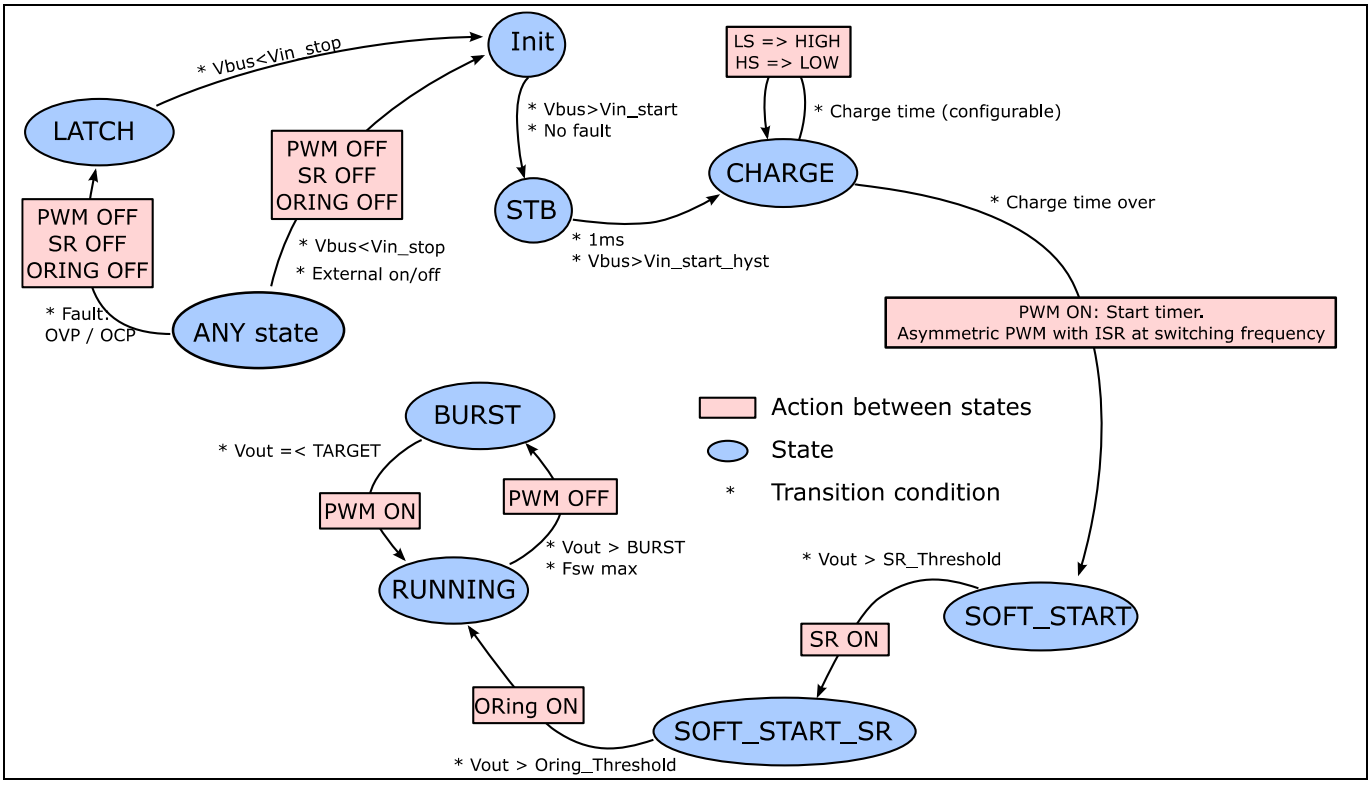


Figure 54 State machine implemented in the LLC control for EVAL_1K6W_PSU_G7_DD.

In the state_control() function, the external on-off functionality is as well integrated, together with the start-stop control according to the input voltage. It is reminded that the bulk voltage (input voltage for LLC) is sensed in the PFC staged and sent viy UART to the secondary side controller. Figure 55 and Figure 56 show a detailed flow diagram of the state_control() function.

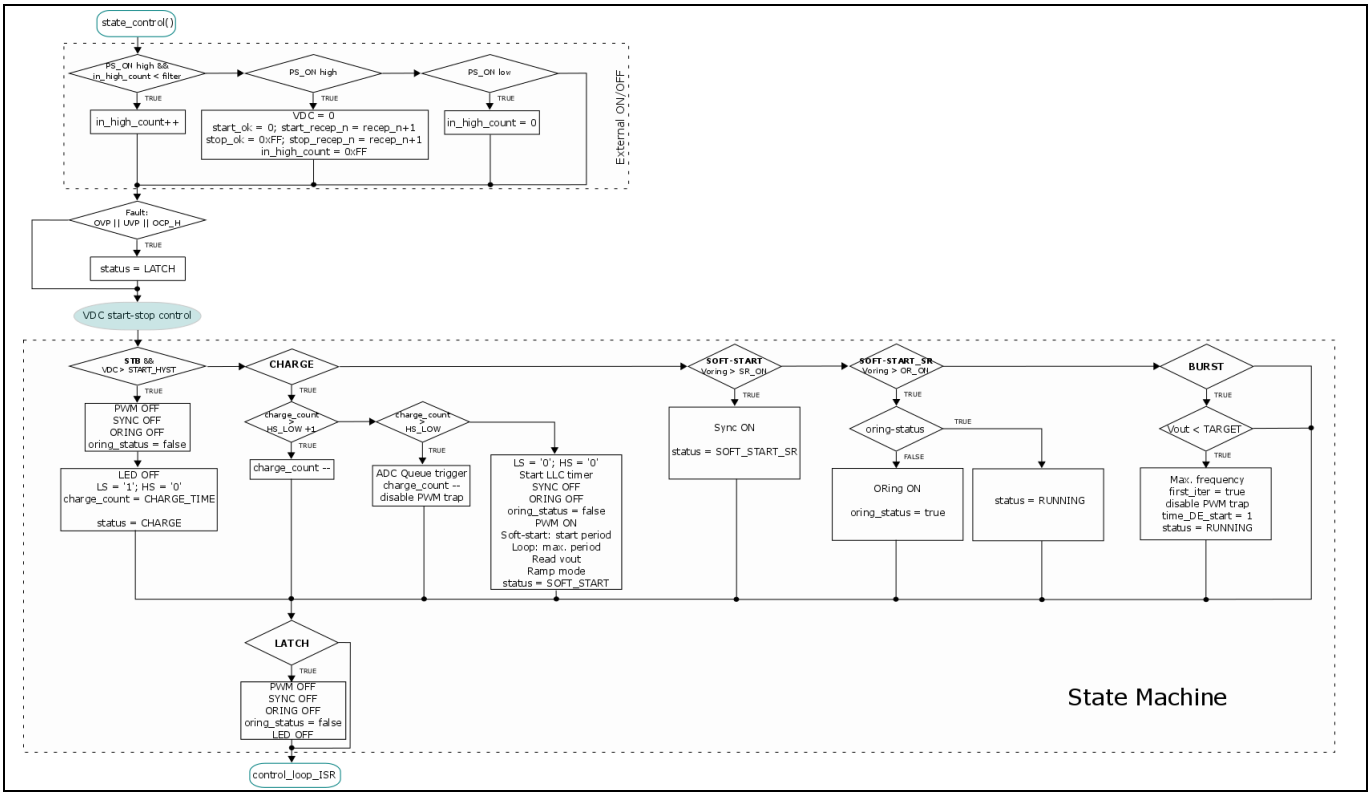


Figure 55 State_control() flow diagram with the external on/off, bulk voltage start-stop and state machine functionalities.

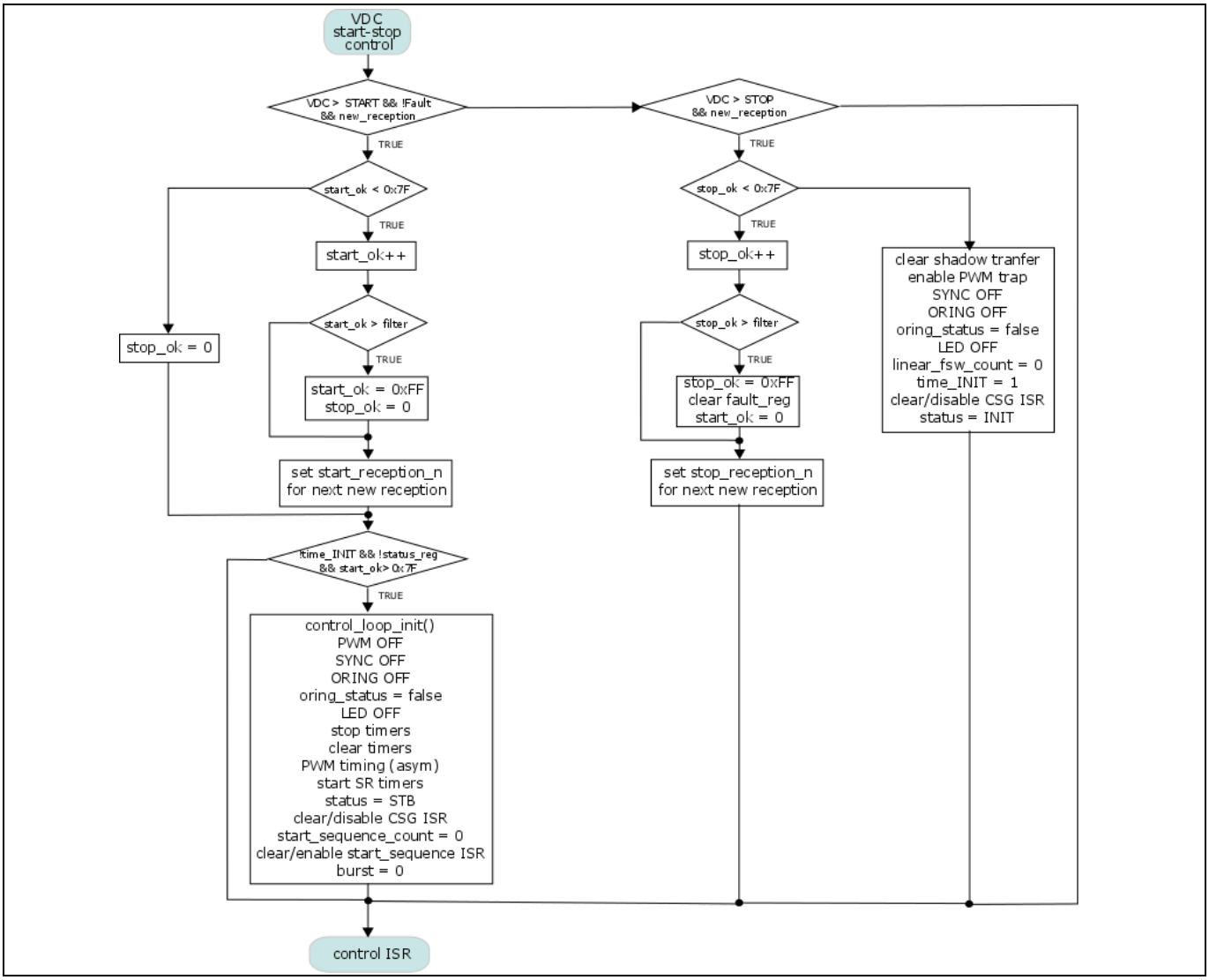


Figure 56 Bulk voltage start-stop flow diagram.

4.4 Voltage loop

The LLC stage of the EVAL_1K6W_PSU_G7_DD board is voltage controlled by a PID controller, Vloop() in Figure 57, which modifies the switching frequency according to the sensed voltage error. In addition to the PID itself, other functions have been implemented for an optimized steady-state ripple and fast transient response. The soft start algorithm is implemented as well in this SW block and a variable dead time according to the switching frequency is included.

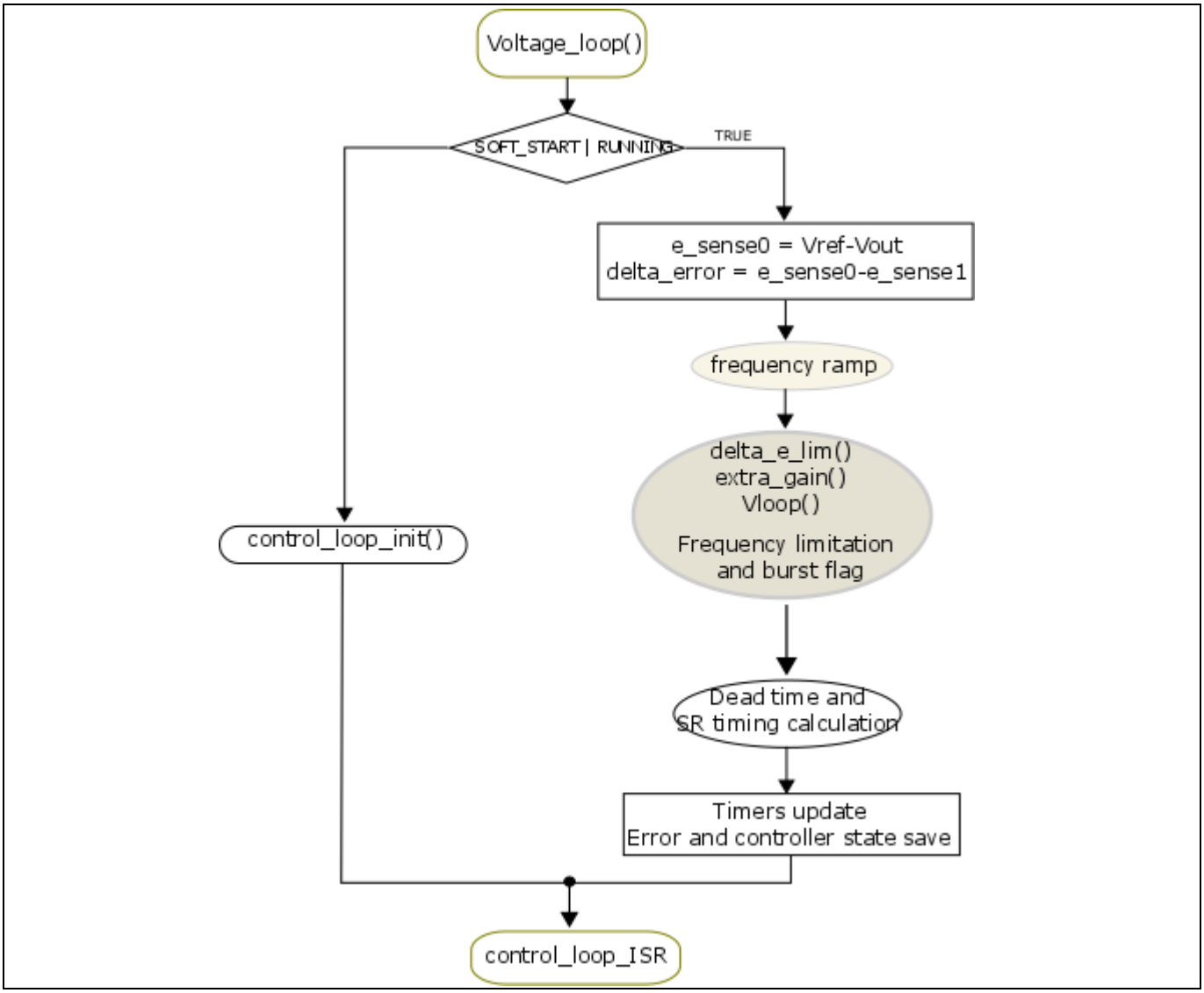


Figure 57 Voltage loop flow diagram.

During start-up, the LLC is operated in open loop and the frequency is linearly decreased, by taking the control period (PR) from a programmed look up table (LUT), in order to increase the output voltage.

During this open loop operation, the voltage control loop starts in the minimum programmed frequency and runs in parallel calculating the required period to get to the output voltage target. Two conditions are considered in order to change to closed loop operation: the voltage error is under a defiend limit, i.e. the output voltage is close to the expected voltage target, or the frequency calculated by the control loop is higher than the one taken from the soft-start programmed ramp.

Figure 58 shows the flow diagram of the frequency ramp up and the block diagram of the implemented control.

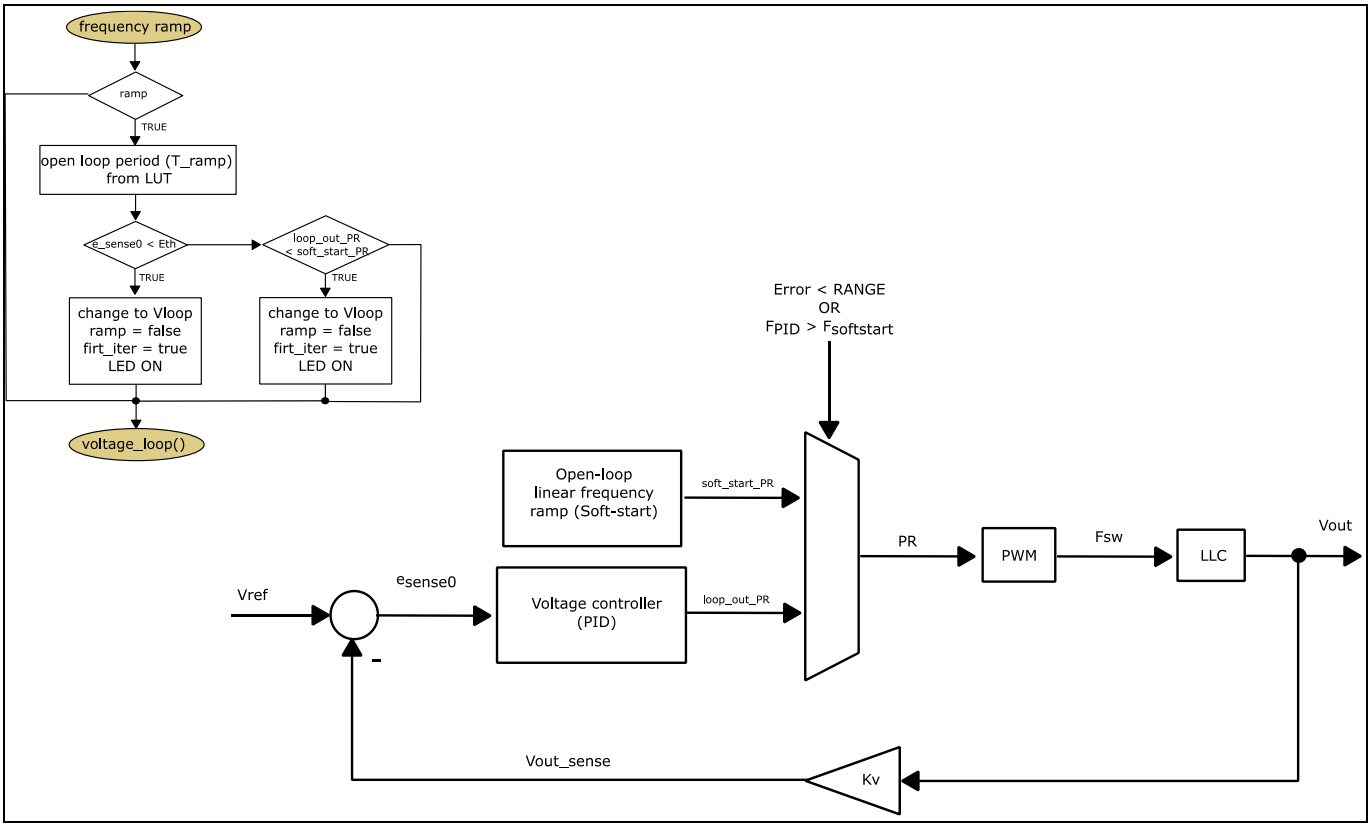


Figure 58 Soft-start concept implemented in the LLC control of the 1600W PSU.

The LLC controller is in charge of keeping the output voltage inside the required dinamyc limits during load or input transients, but also it must guarantee the specified steady-state ripple. The first condition requires a fast control loop with high bandwidth. However, this kind of controller can increase the output voltage ripple in steady state, especially in noisy conditions. Furthermore, the bulk voltage twice line frequency ripple coming from the AC-DC stage can be reflected in the output voltage

Considering all these effects, the following solutions (Figure 59) have been implemented in the LLC controller of the EVAL_1K6W_PSU_G7_DD board.

- The PID coefficients are designed for a lower BW with a consistent phase margin (PM). Blue line in Figure 60.
- An error management is introduced to limit the noise effects: the variation between two consecutive errors is limited to 50mV.

With this two decisions, the high frequency oscillations due to noise are drastically reduced, achieving a a good middle frequency ripple in steady state. However, the previous points introduce two main limitations:

Since the BW is reduced, the gain at 100/120Hz is reduced as well. The gain reduction has a negative impact in the 100/120Hz bulk voltage ripple rejection, since this is inversely proportional to the loop gain at that frequency. An extra gain at low frequencies has been inserted in the controller stage to reduce the low frequency ripple rejection. This gain is shown in the green line of Figure 60.

On the other hand, the differential error limitation introduces a dinamyc response limitation due to the inherent low pass filter effect of this implementation. Error band detection, based on the error absolute value, is introduced to counteract the filter effect. If the error is detected outside this band, extra gain is introduced by shifting the controller intermediate result, as shown in Figure 59. The gain effect in the control frequency response can be seen in Figure 60.

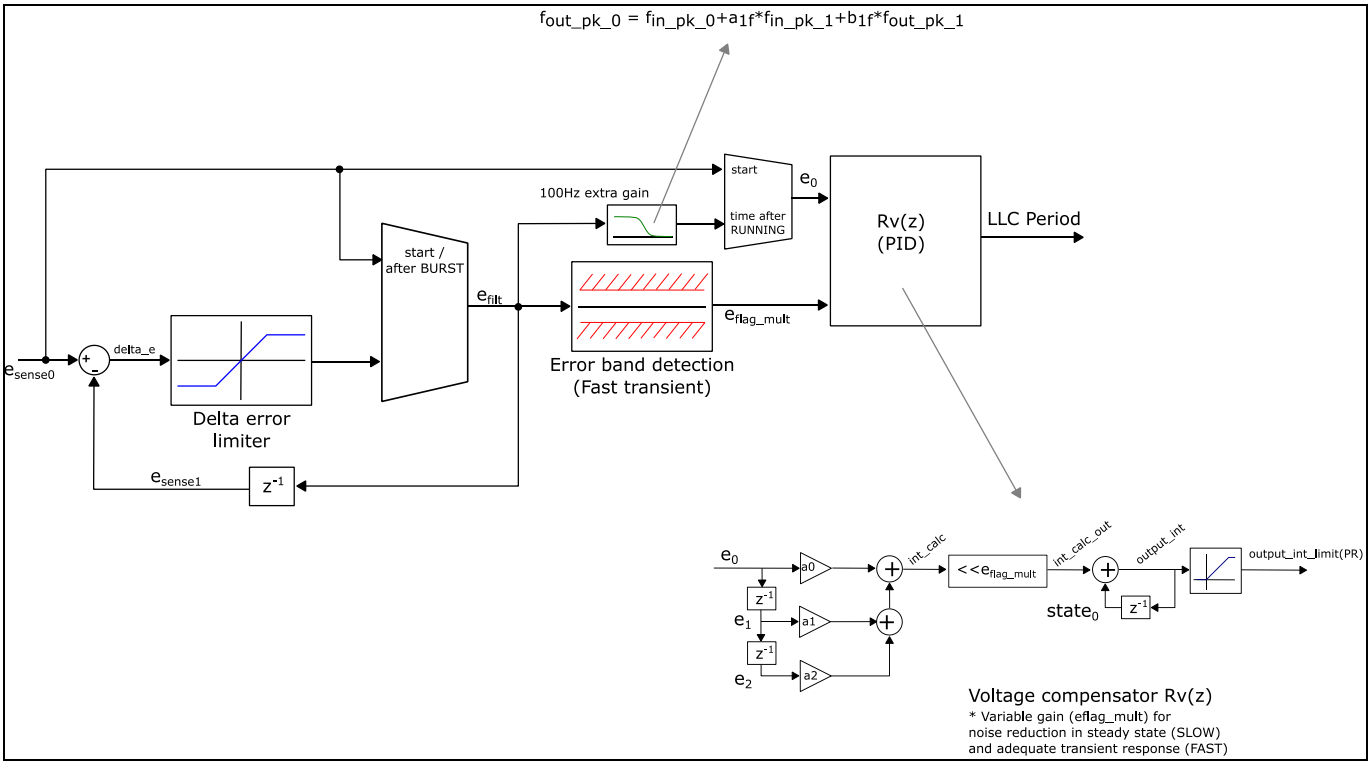


Figure 59 Implementation of the voltage controller block of Figure 58.

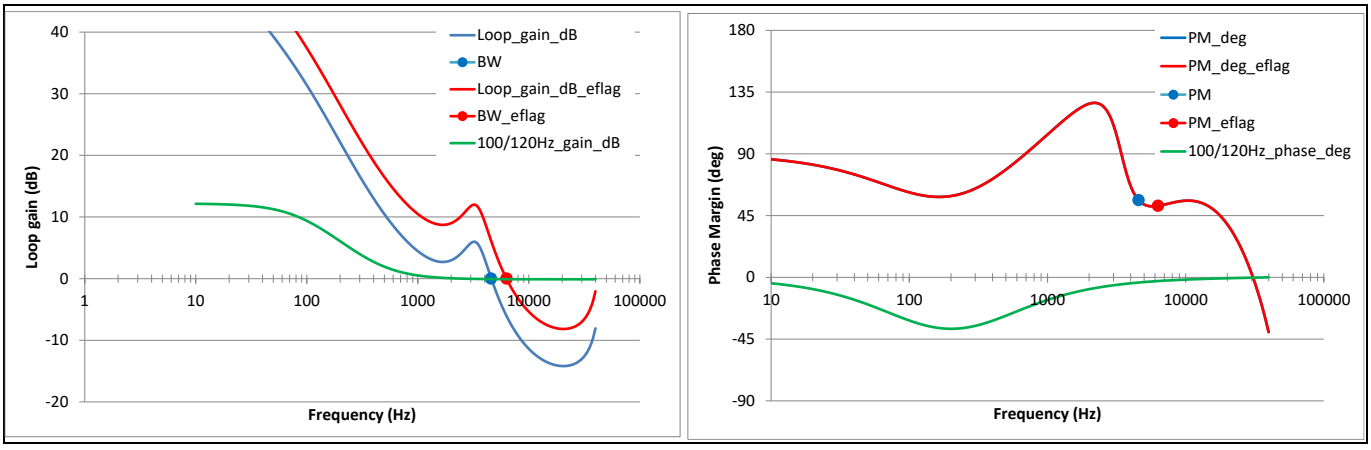


Figure 60 Loop gain of the LLC at nominal operating conditions without (blue) and with (red) extra gain outside the band error. In both cases the low frequency gain increase (green) is applied.

More detail on the implementation can be appreciated in the flow diagram presented in Figure 61. In this same figure the switching frequency limitation and the burst flag management is introduced as well.

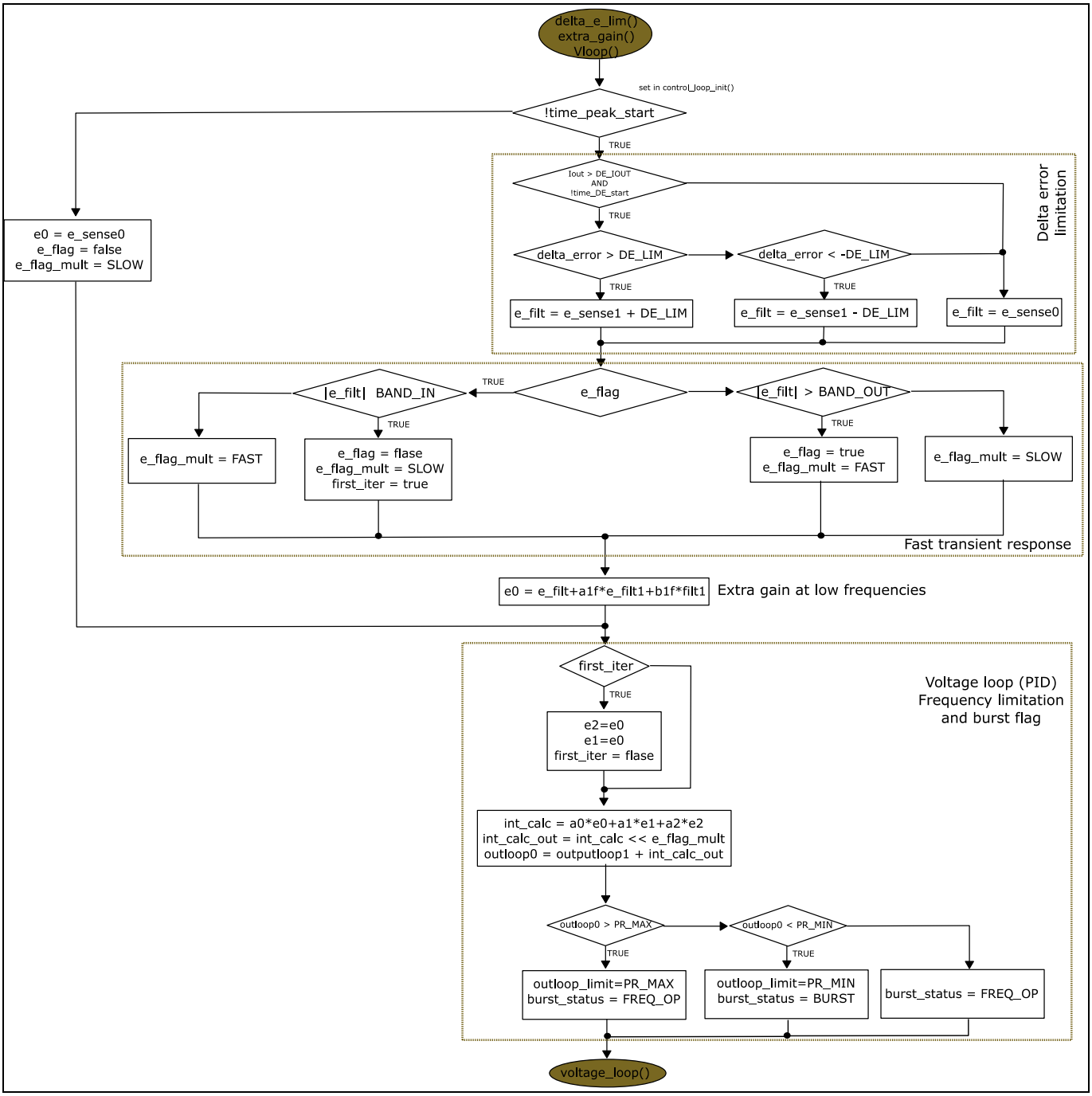


Figure 61 Voltage loop function flow diagram.

As a last action taken in the voltage loop functionality block, the variable half-bridge dead time and SR timing are modified according to the calculated operation period by the voltage loop equation.Figure 62 shows the variable dead time applied in the half-bridge PWM generation for the 1600W LLC.

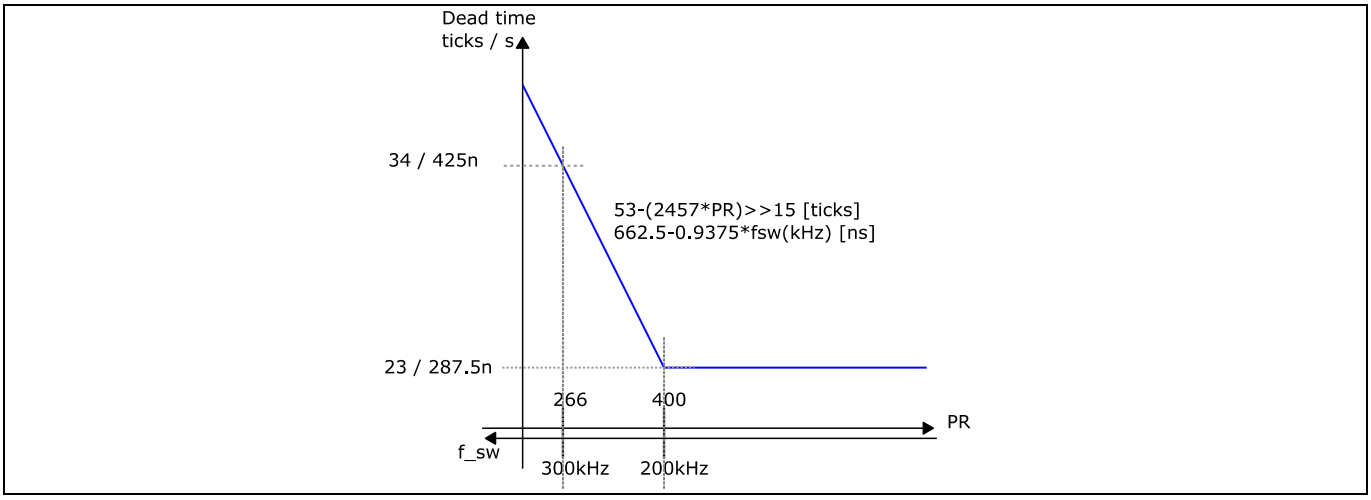


Figure 62 Variable dead time according to the calculated switching period/frequency.

4.5 Burst mode detection

The burst flag set in the frequency limitation of the control loop, together with the output voltage level is used to decide wether start burst mode operation or not. A filter of the condition is introduced to minimiza the burst operation mistriggering. In burst mode operation a special operation with SR active protected by patent is applied. The decision to leave burst mode operation and return to normal frequency control is taken in the state machine.

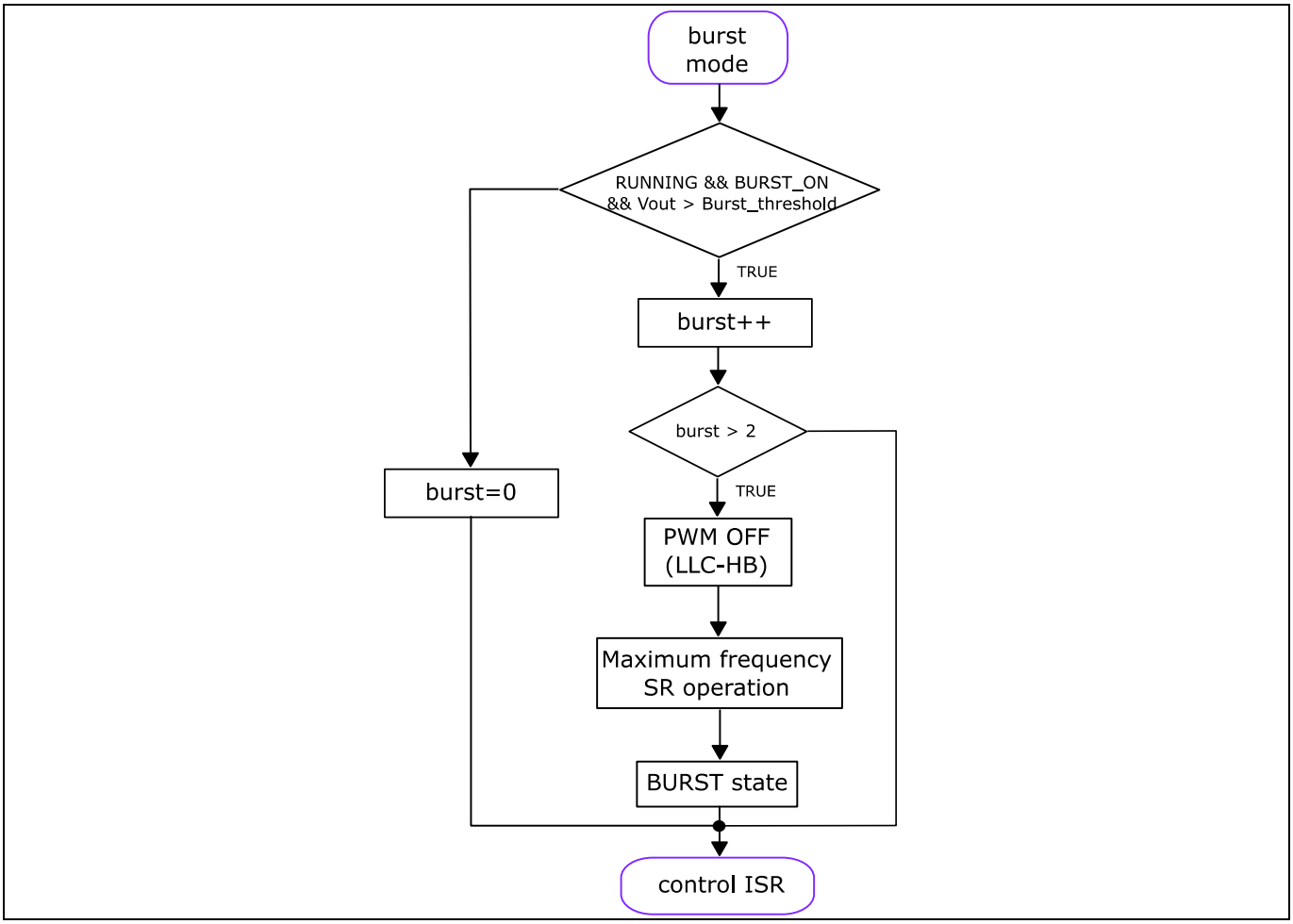


Figure 63 Burst mode detection flow diagram.

4.6 Background processes

Two functions run in the background, outside the main functionality of the control interrupt. These functins are used for counting time of different events happening in the control ISR and for adjustment of the fan speed.

4.6.1 Time counter

A counting variable at the ISR frequency (80kHz) is used as a base for time counting. Three main time domains are implemented: 100µs, 1ms and 100ms.

In this domains the UART timing, variables related with the error management and overcurrent protections are considered.

4.6.2 Fan control

The fan speed is adjusted every 100ms considering the heatsink temperature sent by the PFC controller and processed in the UART_receive() function of the control ISR. Figure 64 depicts the duty cycle applied to the fan in respect to the received temperature.

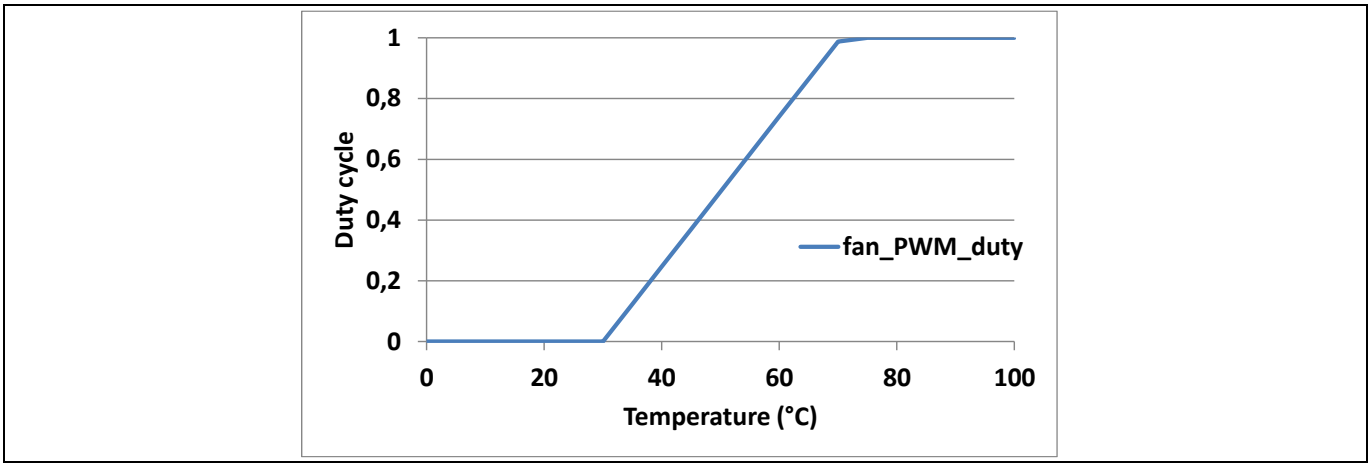


Figure 64 Duty cycle versus temperature applied in EVAL_1K6W_PSU_G7_DD.

5 Summary

This document presents a 1600 W server PSU (EVAL_1K6W_PSU_G7_DD board) which complies with the 80 Plus Titanium efficiency standard: efficiency is over 96 percent at 50 percent load. The achieved power density is 44 W/in^3, which is enabled by the use of SMD packages.

The new DDPAK package is utilized in a power board, which allows reduced commutation loops. Furthermore, the combination of this package with CoolMOS™ G7 and CoolSiC™ G6 diode technologies enables mounting all the semiconductors in the same heatsink and obtains a high power density. In addition, the use of the power board approach will in future enable the testing of new SMD packages, such as QDPAK.

This server PSU also allows the implementation and testing of future Infineon devices and technologies. Further modifications of the power supply shown will be possible by updating different Infineon products such as 2EDF isolated drivers for LLC stage, fifth-generation CoolSET™ in the bias supply or CoolMOS™ S7 as relay replacement. OptiMOS™ 6 information will be available soon. Please check the Infineon website for more information.

6 Schematics

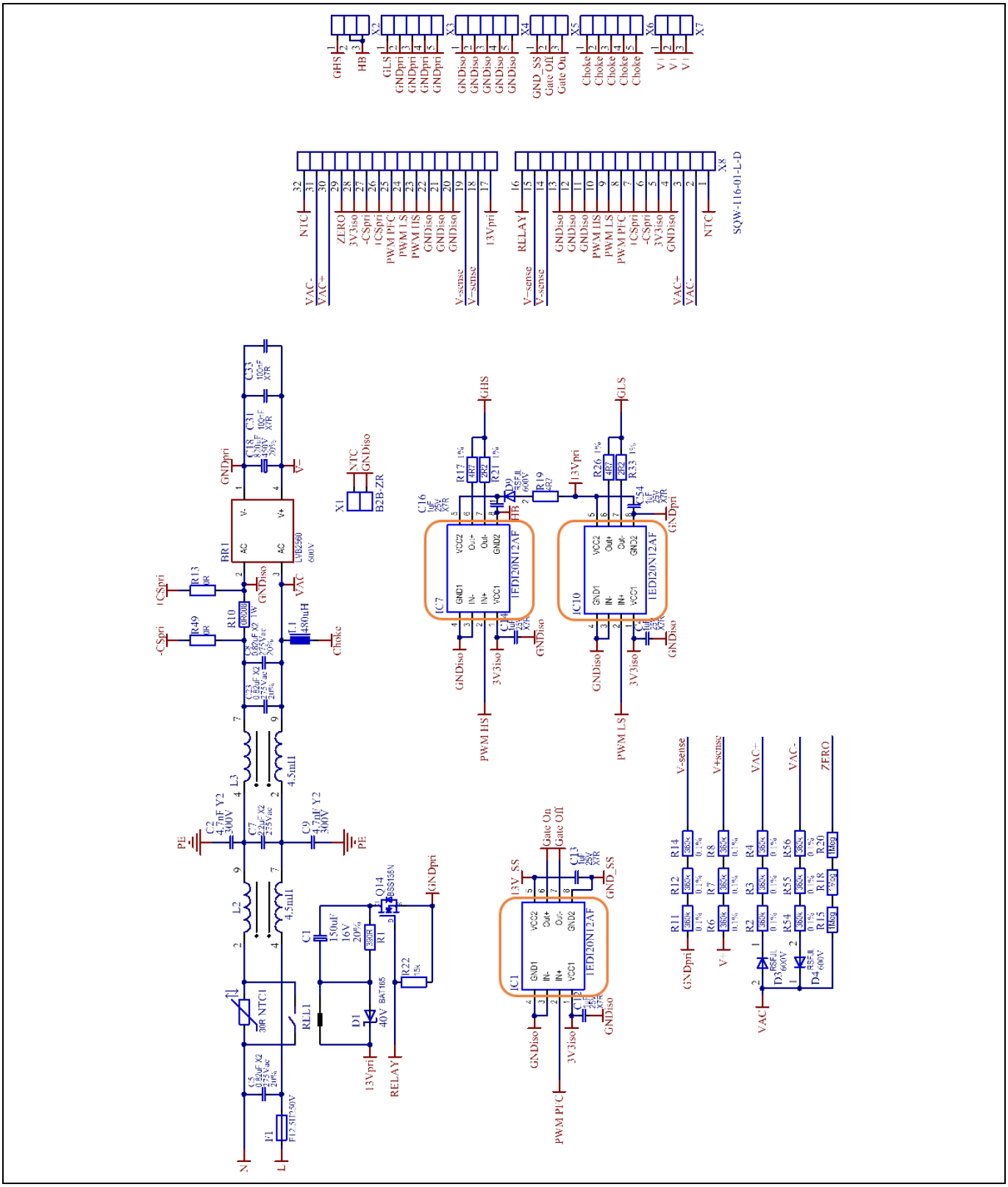


Figure 65 PFC schematic of the 1600 W PSU, which includes the NTC, power board and primary-side control board connectors, as well as the PFC and LLC half-bridge drivers (highlighted in orange). The PFC switch and diode are in the power board.

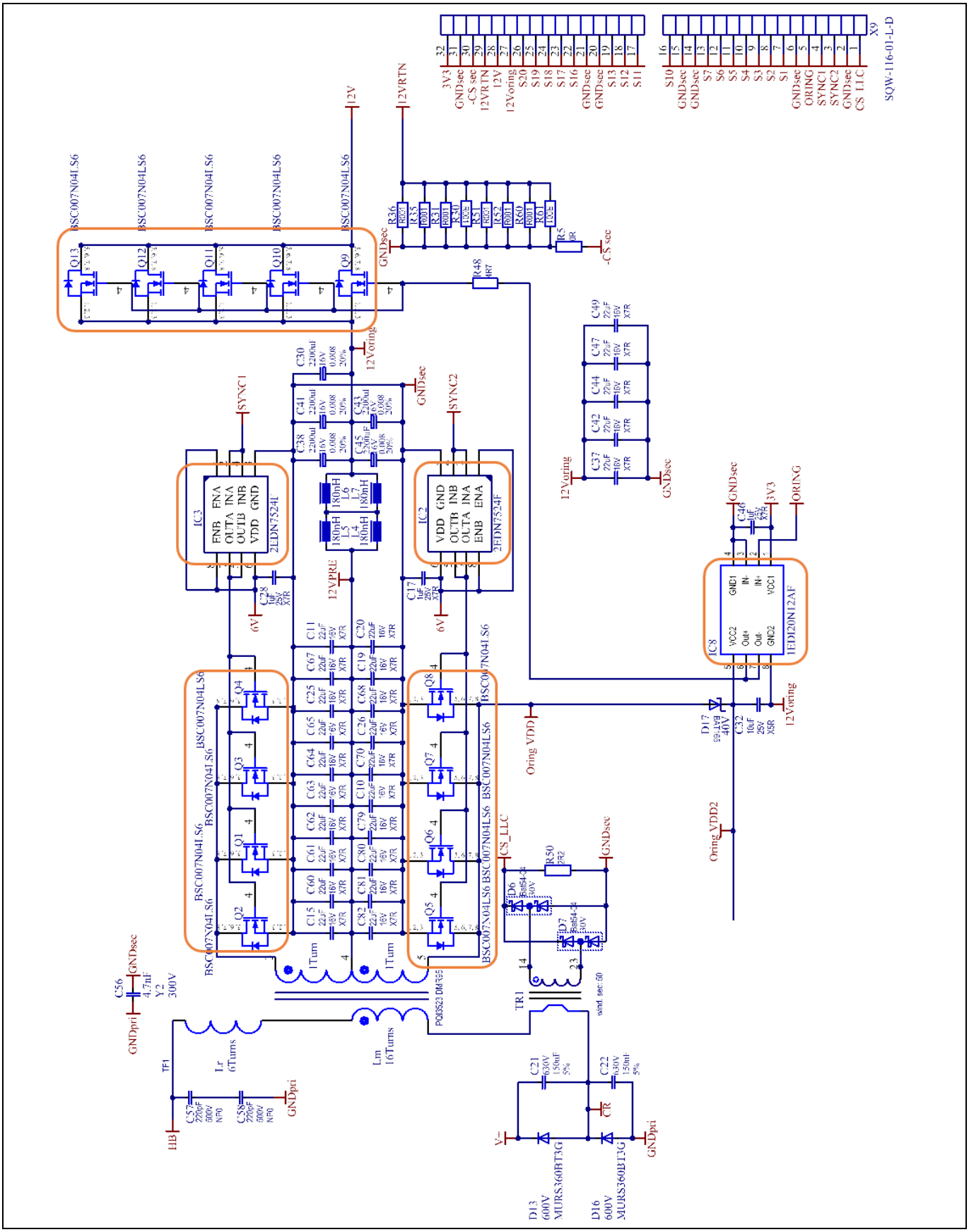


Figure 66 **LLC schematic of the 1600 W PSU with the secondary-side control board connector. The primary-side switches and drivers are in the power board and PFC schematic. Infineon products are highlighted in orange.**

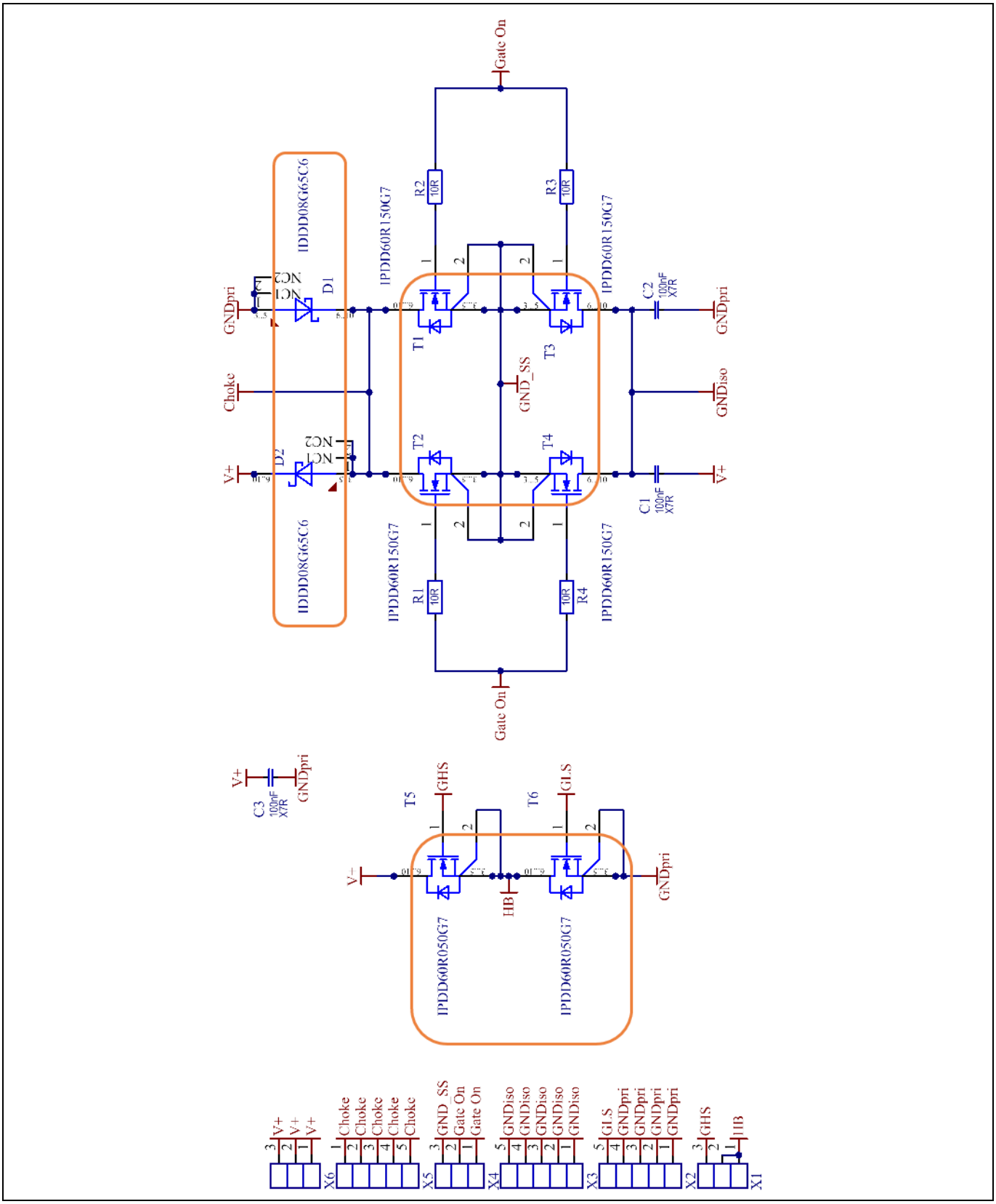


Figure 67 **Power board schematic for the main semiconductors of the 1600 W server PSU. The highlighted parts are the Infineon DDPAK MOSFETs and diodes.**

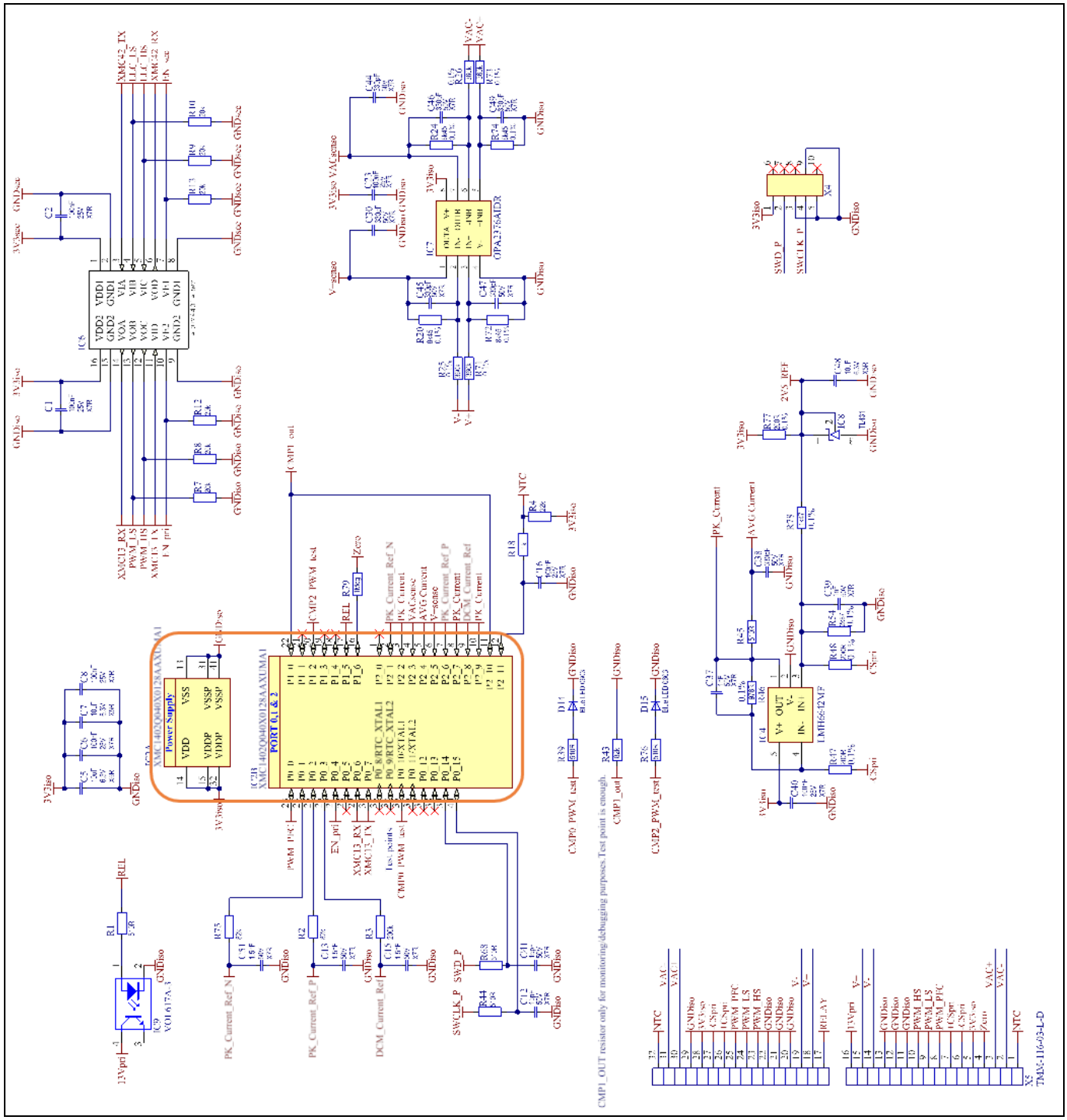


Figure 68 Primary-side controller (XMC1402 highlighted) schematic, including the digital isolator for primary-secondary communication.

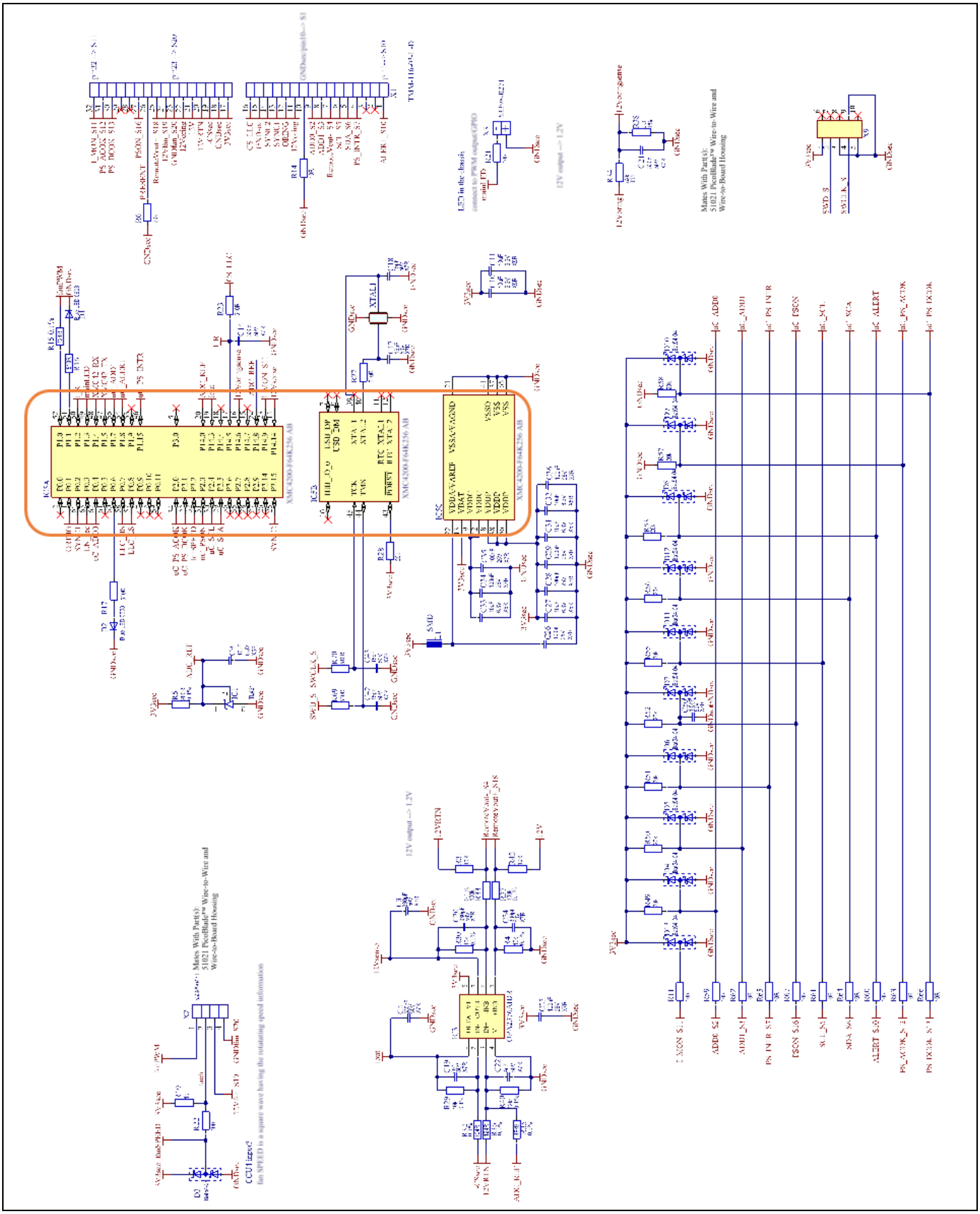


Figure 69 **Secondary-side controller (XMC4200 highlighted) schematic, including the signaling for the PSU output connector.**

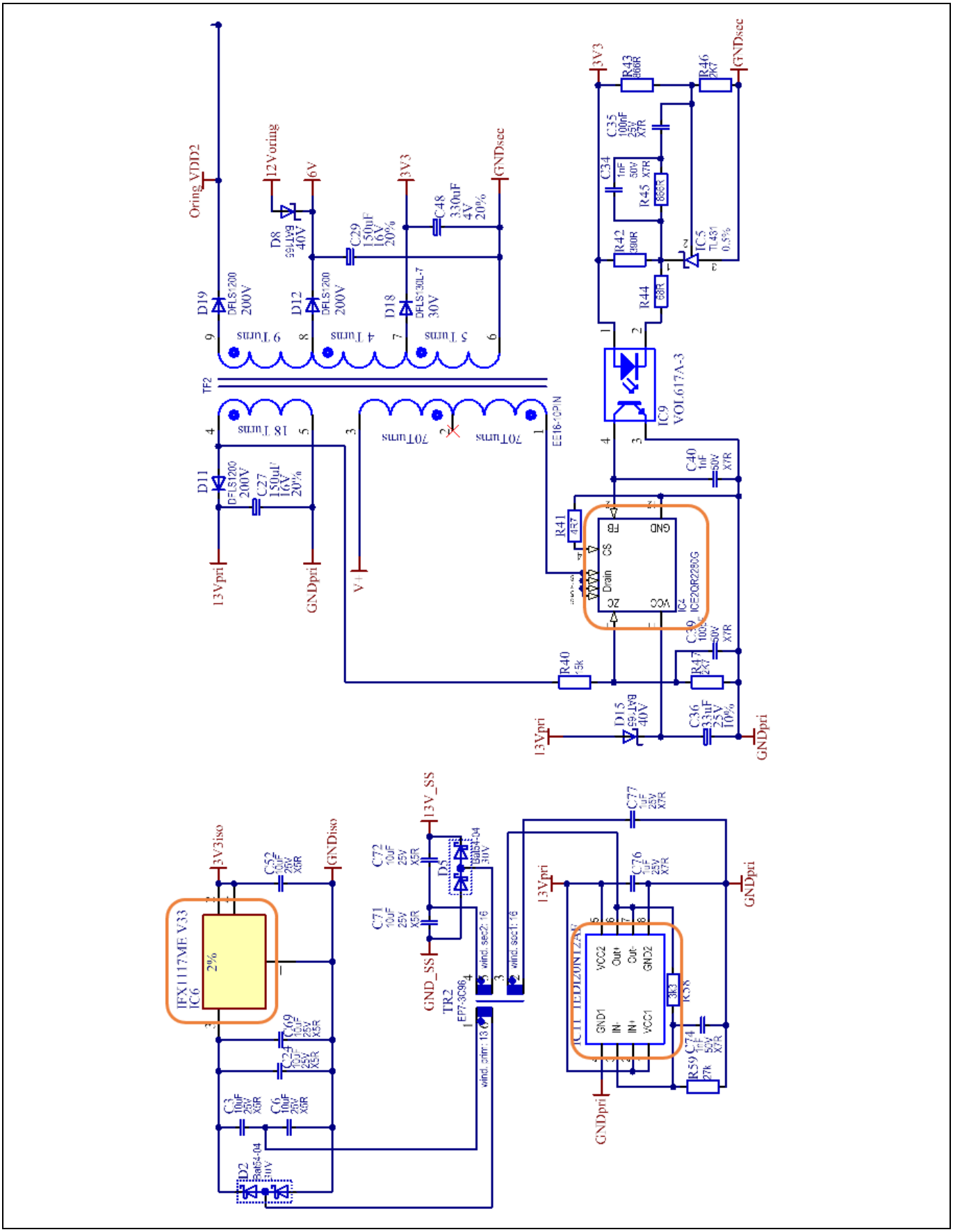


Figure 70 **Auxiliary power supply (bias) of the 1600 W server PSU. The implemented Infineon components are highlighted in orange.**

7 Bill of Materials (BoM)

Table 4 Main board components

Designator	Value	Tolerance	Voltage	Description	Comment
IC2, IC3	**2EDN7524F**			**Integrated circuit**	**SMD**
IC1, IC7, IC8, IC10, IC11	**1EDI20N12AF**			**Integrated circuit**	**SMD**
IC4	**ICE2QR2280G**			**Integrated circuit**	**SMD**
IC6	**IFX1117ME V33**	**2 percent**	**15 V**	**Integrated circuit**	**SMD**
NTC1	30 R	20 percent		NTC resistor	THT
R1	390 R	1 percent		Resistor	SMD
R10	0R008	1 percent		Resistor	SMD
R42	390 R	1 percent		Resistor	SMD
R44	68 R	1 percent		Resistor	SMD
R58	3k3	1 percent		Resistor	SMD
R59	27 k	1 percent		Resistor	SMD
R2, R3, R4, R6, R7, R8, R11, R12, R14, R54, R55, R56	360 k	0.1 percent		Resistor	SMD
R22, R40	15 k	1 percent		Resistor	SMD
R43, R45	866 R	1 percent		Resistor	SMD
R46, R47	2K7	1 percent		Resistor	SMD
R15, R18, R20	1 Meg	1 percent		Resistor	SMD
R21, R33, R50	2R2	1 percent		Resistor	SMD
R5, R13, R49	0 R	1 percent		Resistor	SMD
R17, R19, R26, R41, R48	4R7	1 percent		Resistor	SMD
R30, R31, R35, R36, R51, R52, R60, R61	R001	1 percent		Resistor	SMD
REL1	OJE-SS-112HM		12 V	Relay	THT
Q14	BSS138N		60 V	MOSFET	SMD
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13	BSC007N04LS6		40 V	MOSFET	SMD
L1	480 µH			Magnetic	THT
TF1	PQI3523 DMR95			Magnetic	THT
TF2	EE16-10PIN			Magnetic	THT
TR1				Magnetic	THT
TR2	EP7-3C96			Magnetic	THT
L2, L3	4.5 mH			Magnetic	THT
L4, L5, L6, L7	180 nH			Magnetic	SMD
IC5	TL431	0.5 percent		Integrated circuit	SMD
IC9	VOL617A-3			Integrated circuit	SMD
F1	F12.5H250V			Fuse	THT
D1, D8, D15, D17	BAT165		40 V	Schottky diode	SMD
D2, D5, D6, D7	BAT54-04		30 V	Schottky diode	SMD
BR1	LVB2560		600 V	Bridge diode	THT
D18	DFLS130L-7		30 V	Diode	SMD
D13, D16	MURS360BT3G		600 V	Diode	SMD
D11, D12, D19	DFLS1200		200 V	Diode	SMD
D3, D4, D9	RSFJL		600 V	Diode	SMD
X1	B2B-ZR			Connector	THT
X8, X9	SQW-116-01-L-D			Connector	THT
C18	820 µF	20 percent	450 V	Polarized capacitor	THT

Designator	Value	Tolerance	Voltage	Description	Comment
C36	33 µF	10 percent	25 V	Polarized capacitor	SMD
C48	330 µF	20 percent	4 V	Polarized capacitor	SMD
C1, C27, C29	150 µF	20 percent	16 V	Polarized capacitor	SMD
C30, C38, C41, C43, C45	2200 µF	20 percent	16 V	Polarized capacitor	THT
C7	2.2 µF X2	20 percent	275 V AC	Foil capacitor	THT
C21, C22	150 nF	5 percent	630 V	Foil capacitor	THT
C5, C8, C23	0.82 µF X2	20 percent	275 V AC	Foil capacitor	THT
C35	100 nF	X7R	25 V	Ceramic capacitor	SMD
C39	100 pF	X7R	50 V	Ceramic capacitor	SMD
C4, C12, C13, C14, C16, C17, C28, C46, C54, C76, C77	1 µF	X7R	25 V	Ceramic capacitor	SMD
C31, C33	100 nF		500 V	Ceramic capacitor	SMD
C57, C58	220 pF	NP0	500 V	Ceramic capacitor	SMD
C10, C11, C15, C19, C20, C25, C26, C37, C42, C44, C47, C49, C60, C61, C62, C63, C64, C65, C67, C68, C70, C79, C80, C81, C82	22 µF	X7R	16 V	Ceramic capacitor	SMD
C2, C9, C56	4.7 nF	Y2	300 V	Ceramic capacitor	THT
C34, C40, C74	1 nF	X7R	50 V	Ceramic capacitor	SMD
C3, C6, C24, C32, C52, C69, C71, C72	10 µF	X5R	25 V	Ceramic capacitor	SMD

Table 5 Power board components

Designator	Value	Tolerance	Voltage	Description	Comment
T5, T6	**IPDD60R050G7**			**600 V CoolMOS™ G7 power transistor, 600 V (VDS)**	**SMD**
T1, T2, T3, T4	**IPDD60R150G7**			**600 V CoolMOS™ G7 power transistor, 600 V (VDS)**	**SMD**
D1, D2	**IDDD08G65C6**			**650 V CoolSiC™ G6 Schottky diode**	**SMD**
R1, R2, R3, R4	10 R	1 percent		Resistor	SMD
C1, C2, C3	100 nF		500 V	Ceramic capacitor	SMD
X1, X4, X6	MMT-103-01-L-SH			Connector	SMD
X2, X3, X5	MMT-105-01-L-SH			Connector	SMD

Table 6 Control board components

Designator	Value	Tolerance	Voltage	Description	Comment
IC2	**XMC1402-Q040X0128AAXUMA1**			**Integrated circuit**	**SMD**
IC5	**XMC4200-F64K256AB**			**Integrated circuit**	**SMD**
C1, C2, C6, C8, C16, C23, C25, C26, C28, C29, C34,	100 nF	X7R	25 V	Ceramic capacitor	SMD

Bill of Materials (BoM)

Designator	Value	Tolerance	Voltage	Description	Comment
C35, C36, C40					
C3, C4, C14, C20, C21, C24, C30, C38, C44, C45, C46, C47, C49	330 pF	X7R	50 V	Ceramic capacitor	SMD
C5, C7, C9, C10, C11, C27, C31, C32, C33, C48	10 µF	X5R	6.3 V	Ceramic capacitor	SMD
C12, C17, C18, C41, C42, C43	15 pF	X7R	50 V	Ceramic capacitor	SMD
C13, C15, C50, C51	1.5 nF	X7R	50 V	Ceramic capacitor	SMD
C19, C22	4 n7	X7R	50 V	Ceramic capacitor	SMD
C37, C39	1 nF	X7R	50 V	Ceramic capacitor	SMD
D1, D2, D14, D15	Blue LED 0603			LED diode	SMD
D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13	BAT54-04			Diode	SMD
IC1, IC8	TL431			Integrated circuit	SMD
IC3, IC7	OPA2376AIDR			Integrated circuit	SMD
IC4	LMH6642MF			Integrated circuit	SMD
IC6	ADUM4401ARWZ			Integrated circuit	SMD
IC9	VOL617A-3			Integrated circuit	SMD
L1	Ferrite bead 60 Ω at 100 mHz			Magnetic	SMD
R1, R16, R17, R23, R27, R39, R44, R45, R68, R69, R70, R76	510 R	1 percent		Resistor	SMD
R2, R34, R43, R75	82 k	1 percent		Resistor	SMD
R3	200 k	1 percent		Resistor	SMD
R4	22 k	1 percent		Resistor	SMD
R5, R47, R48, R77	200 R	0.1 percent		Resistor	SMD
R6, R7, R8, R9, R10, R12, R13, R28, R49, R50, R51, R52, R53, R55, R56, R57, R58	20 k	1 percent		Resistor	SMD
R11, R14, R21, R22, R31, R42, R59, R60, R61, R62, R63, R64, R65, R66, R67	10 R	1 percent		Resistor	SMD
R15, R32, R36	124 R	0.1 percent		Resistor	SMD
R18, R19	1 k	1 percent		Resistor	SMD
R20, R24, R72, R74	8k45	0.1 percent		Resistor	SMD
R25, R26, R71, R73	360 k	0.1 percent		Resistor	SMD
R29, R30, R41	10 k	0.1 percent		Resistor	SMD
R33, R37	100 k	0.1 percent		Resistor	SMD
R35	49k9	0.1 percent		Resistor	SMD
R38	9k1	1 percent		Resistor	SMD
R40	12k4	0.1 percent		Resistor	SMD
R46	976 R	0.1 percent		Resistor	SMD
R54	2k87	0.1 percent		Resistor	SMD
R78	1k47	0.1 percent		Resistor	SMD
R79	1 Meg	1 percent		Resistor	SMD
X1, X5	TMM-116-03-L-D			Connector	SMD

Bill of Materials (BoM)

Designator	Value	Tolerance	Voltage	Description	Comment
X2	53398-0471			Connector	SMD
X3	53398-0271			Connector	SMD
X4, X9				Connector	SMD
XTAL1	12 MHz			Crystal oscillator	SMD

8 References

[1] “800 W Platinum® server power supply, using 600 V CoolMOS™ C7 and digital control with XMC™”. AN_201707_PL52_022.

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Revision history

Major changes since the last revision

Page or reference	Description of change
Section 2	Section 2.7 with thermal measurements added.

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